

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U37C

Clarkfield/Auburndale

DDR SYSTEM MEMORY A

Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

DM signals are not present on Clarkfield
processor. All DM signal can be left as
NC on Clarkfield and connect directly to
GND on So-DIMM side for Clarkfield
design only

U37D

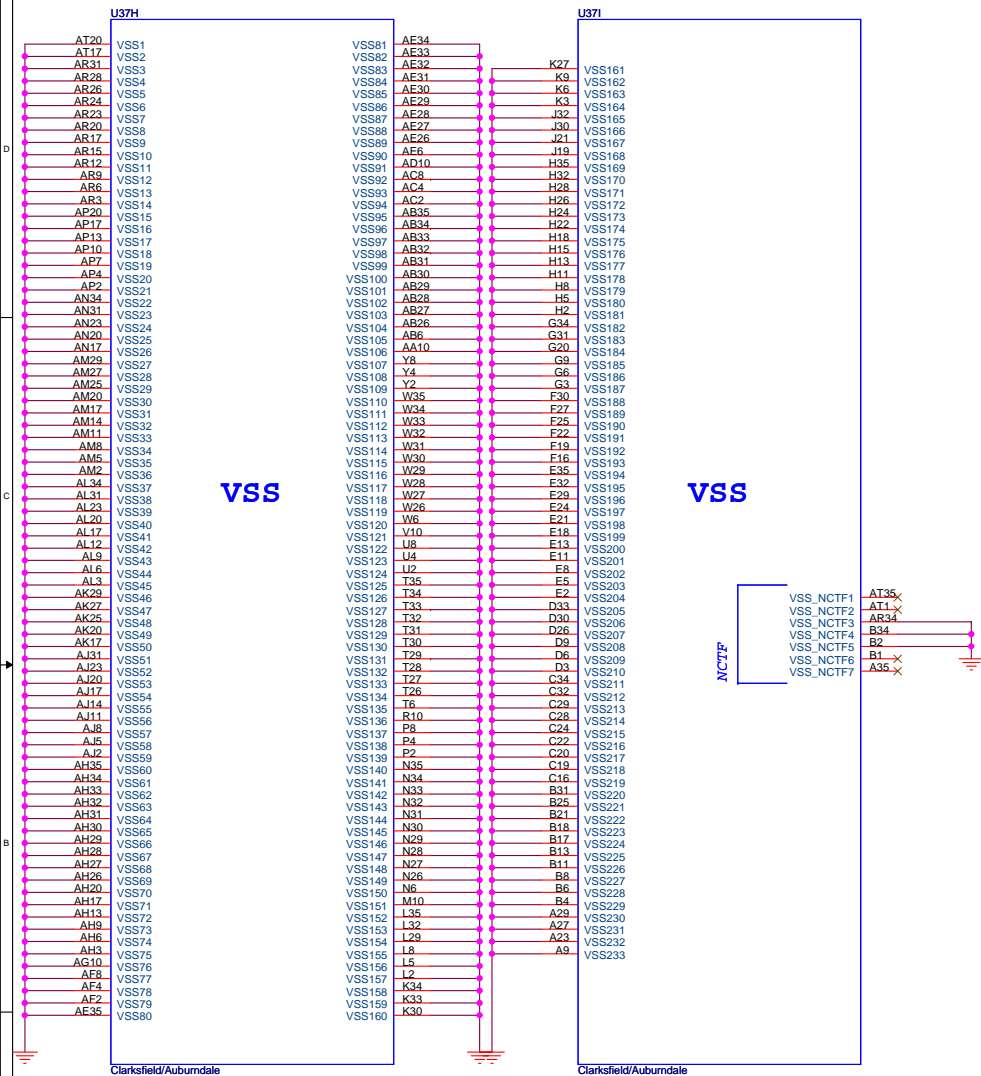
Clarkfield/Auburndale

DDR SYSTEM MEMORY - B

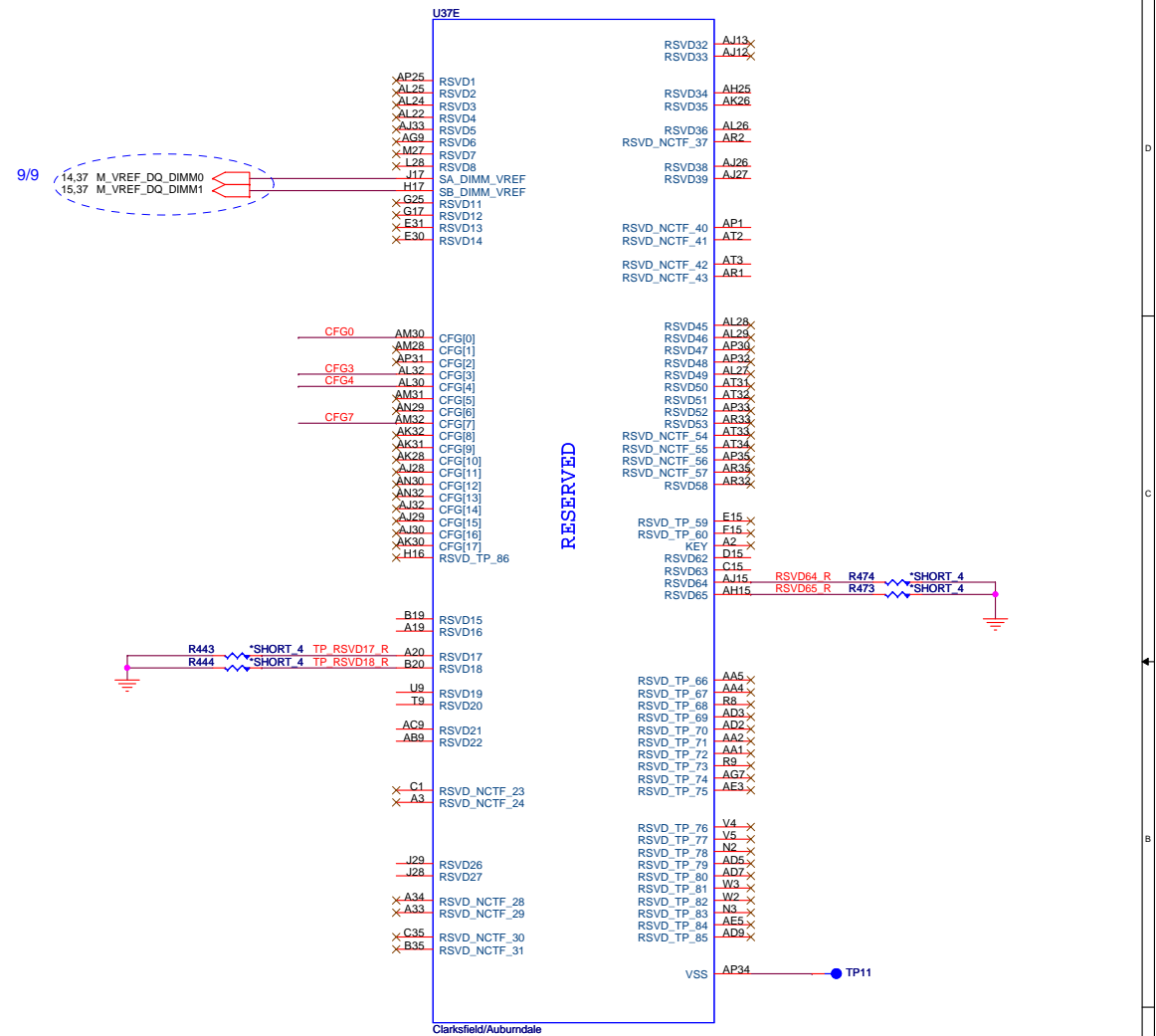
Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)




AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



Processor Strapping

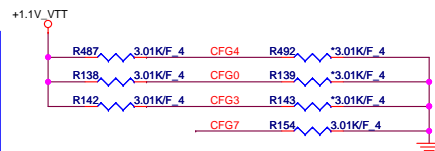
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

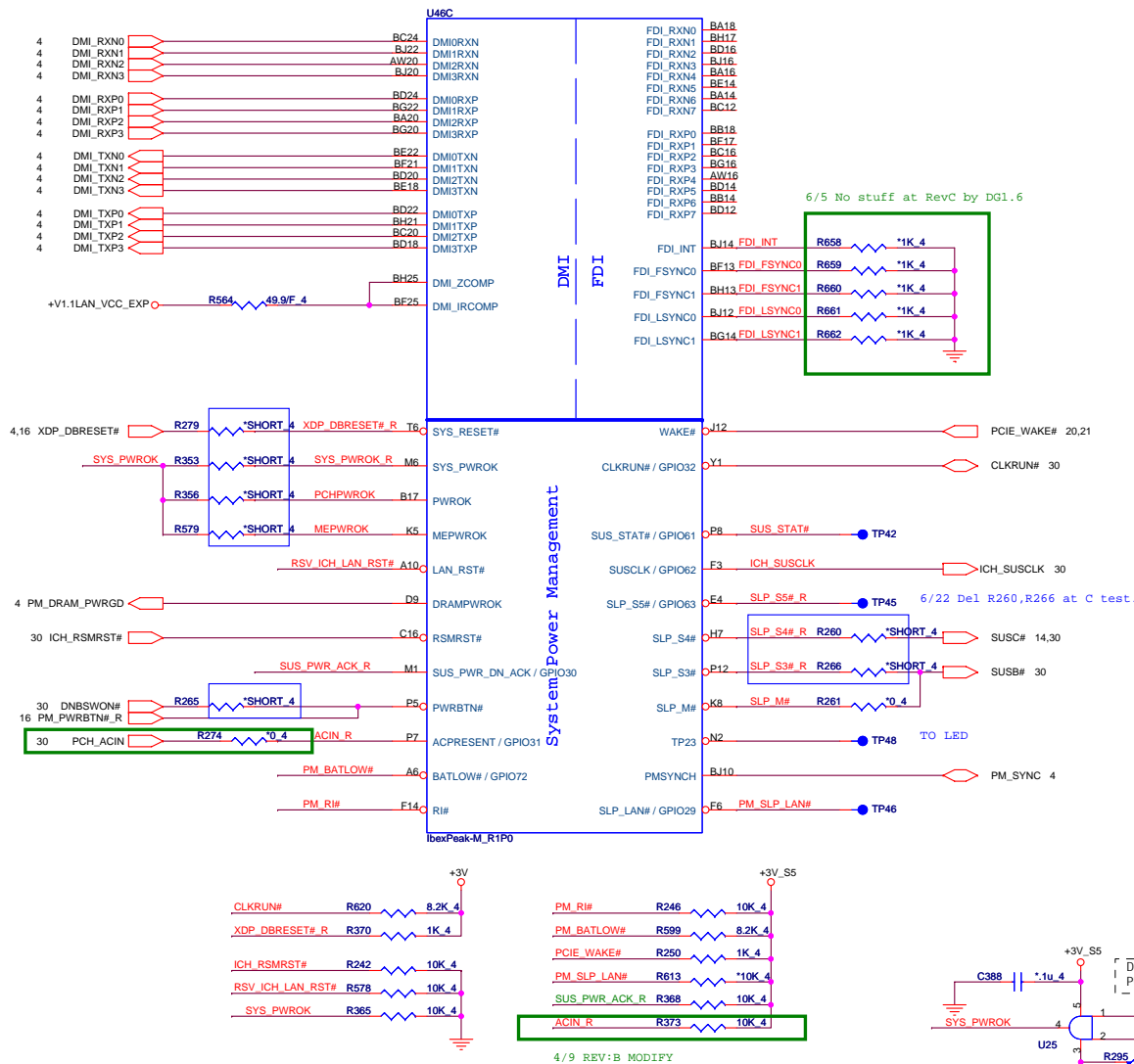
**Quanta Computer Inc.**
PROJECT : ZY9

Size	Document Number	Rev
	AUBURND4 4/4	3A
Date:	Thursday, August 27, 2009	Sheet 7 of 42

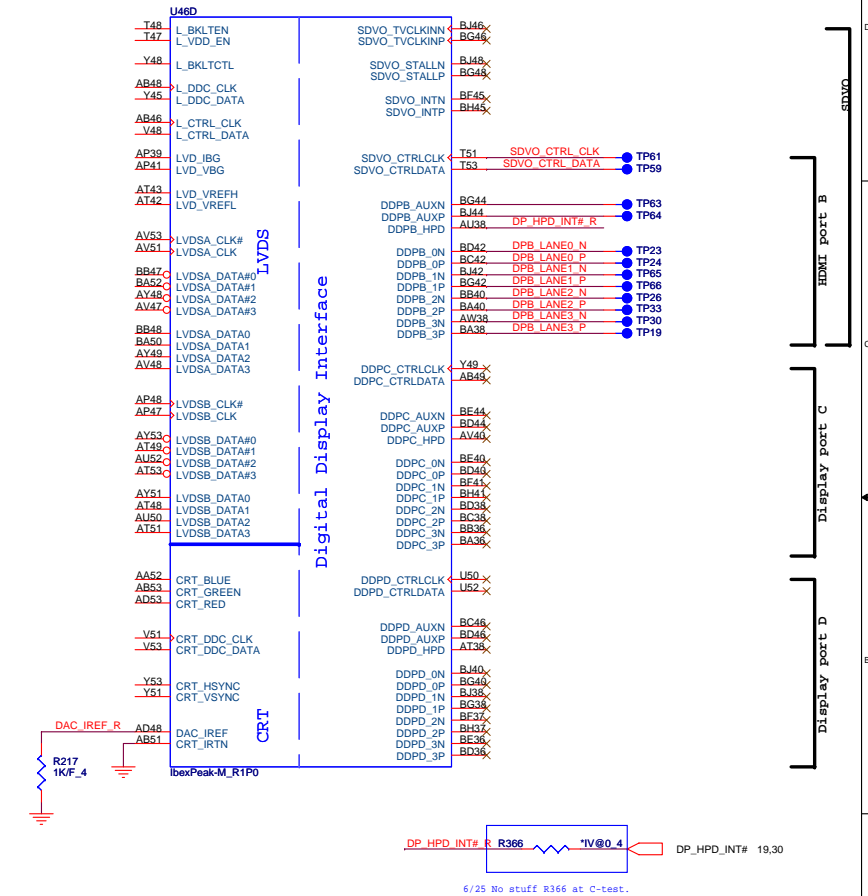
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



IBEX PEAK-M (DMI, FDI, GPIO)



IBEX PEAK-M (LVDS, DDI)



Quanta Computer Inc.

PROJECT : ZY9

Size	Document Number	Rev
	IBEX PEAK-M 1/6	3A
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RTC Circuitry

CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

IBEX PEAK-M (HDA,JTAG,SATA)

INFORMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

7/1 change from +3V_S5 to +3V by intel.

6/21 Non stuff R233 by Intel at C-test.

Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

For PCH 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI

iTPM ENABLE/DISABLE

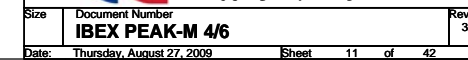
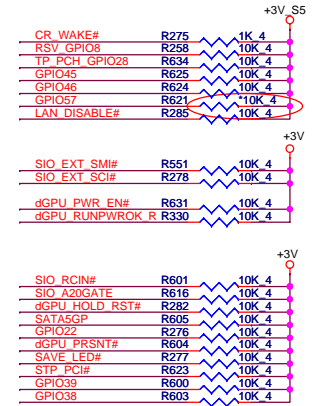
TPM Function	R591
Enable	Mount
Disable	NC (Default)

SATA_DET1# R369 *0.4 dGPU_EDIDSEL# 19

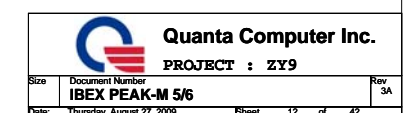
IBEX PEAK-M (PCI-E, SMBUS, CLK)



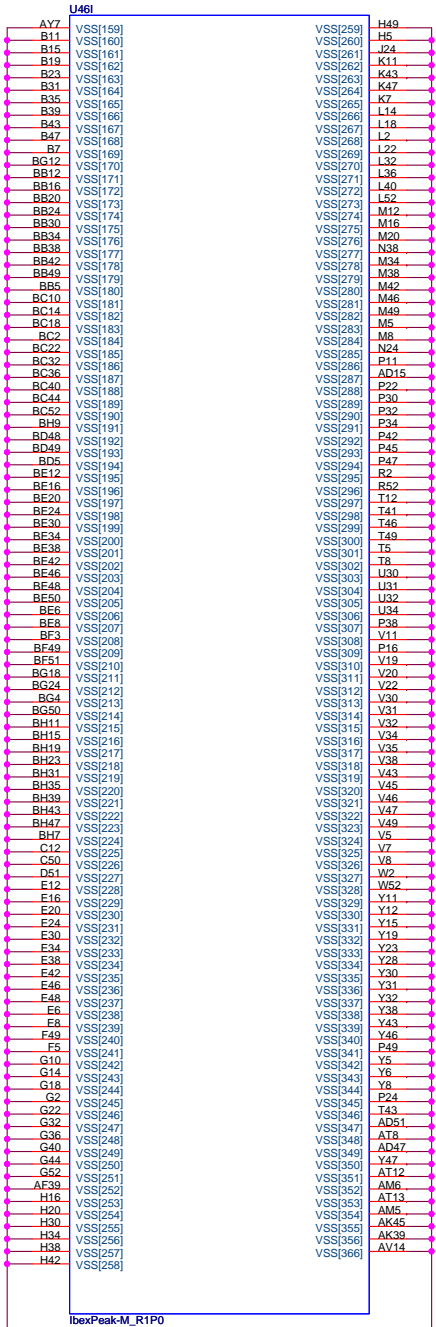
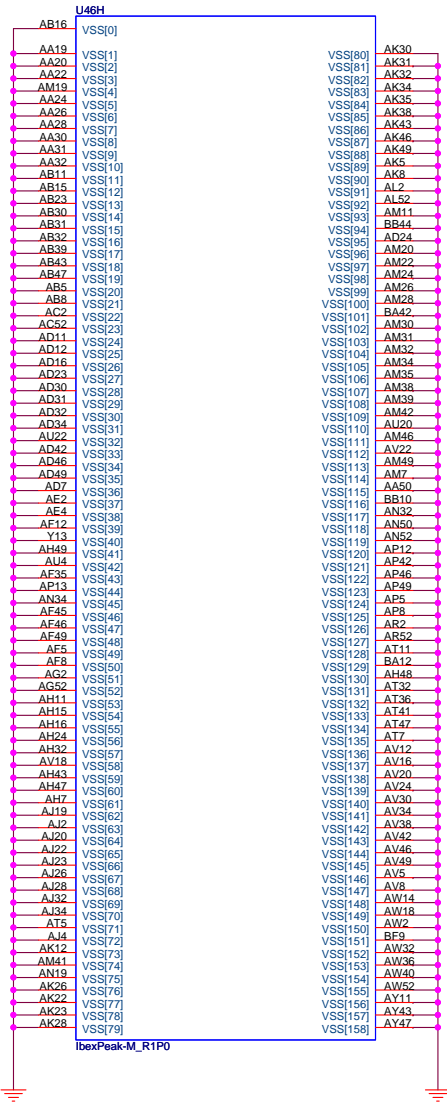
U46F

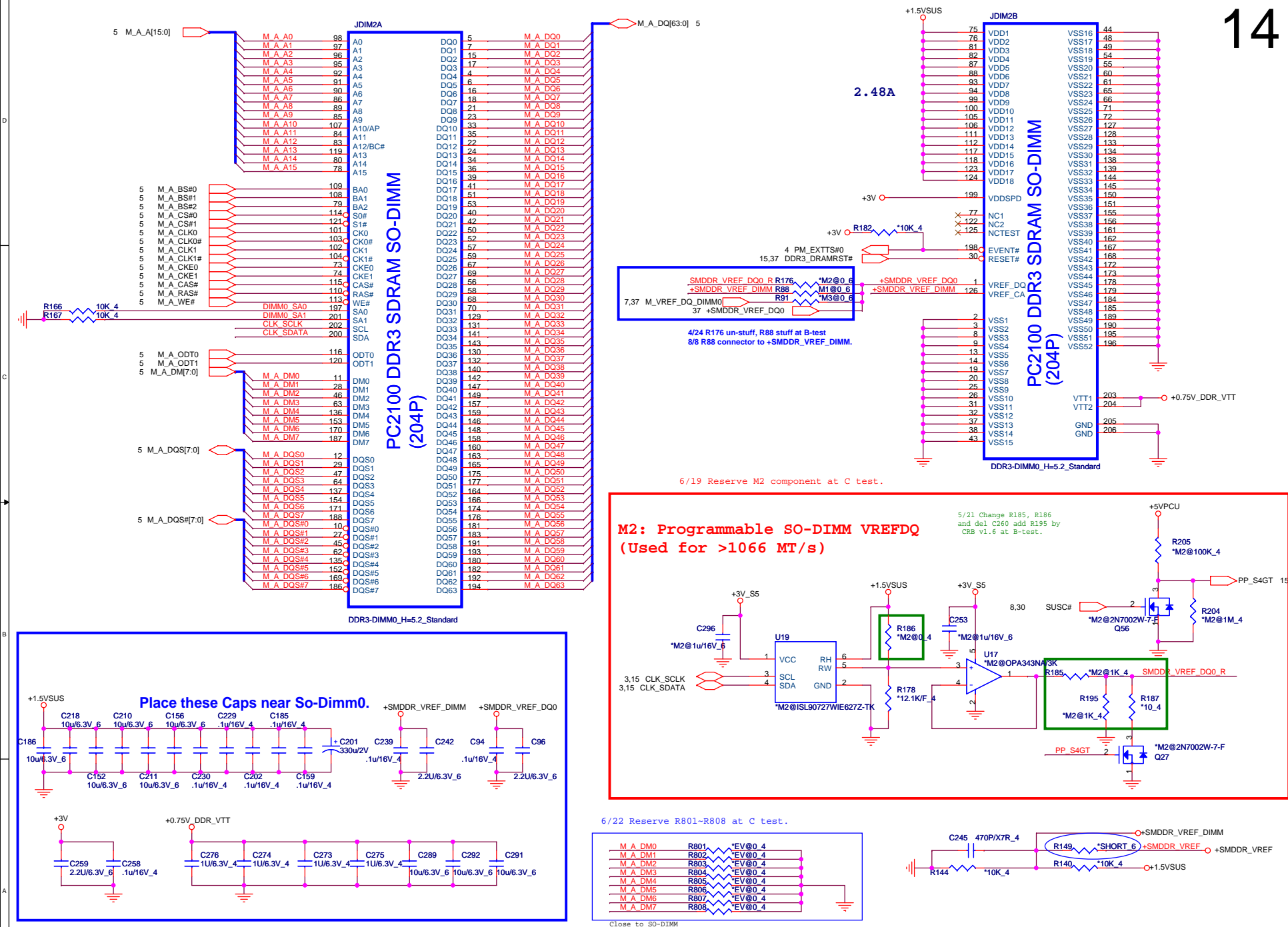


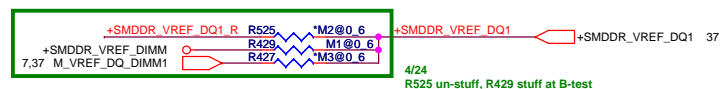
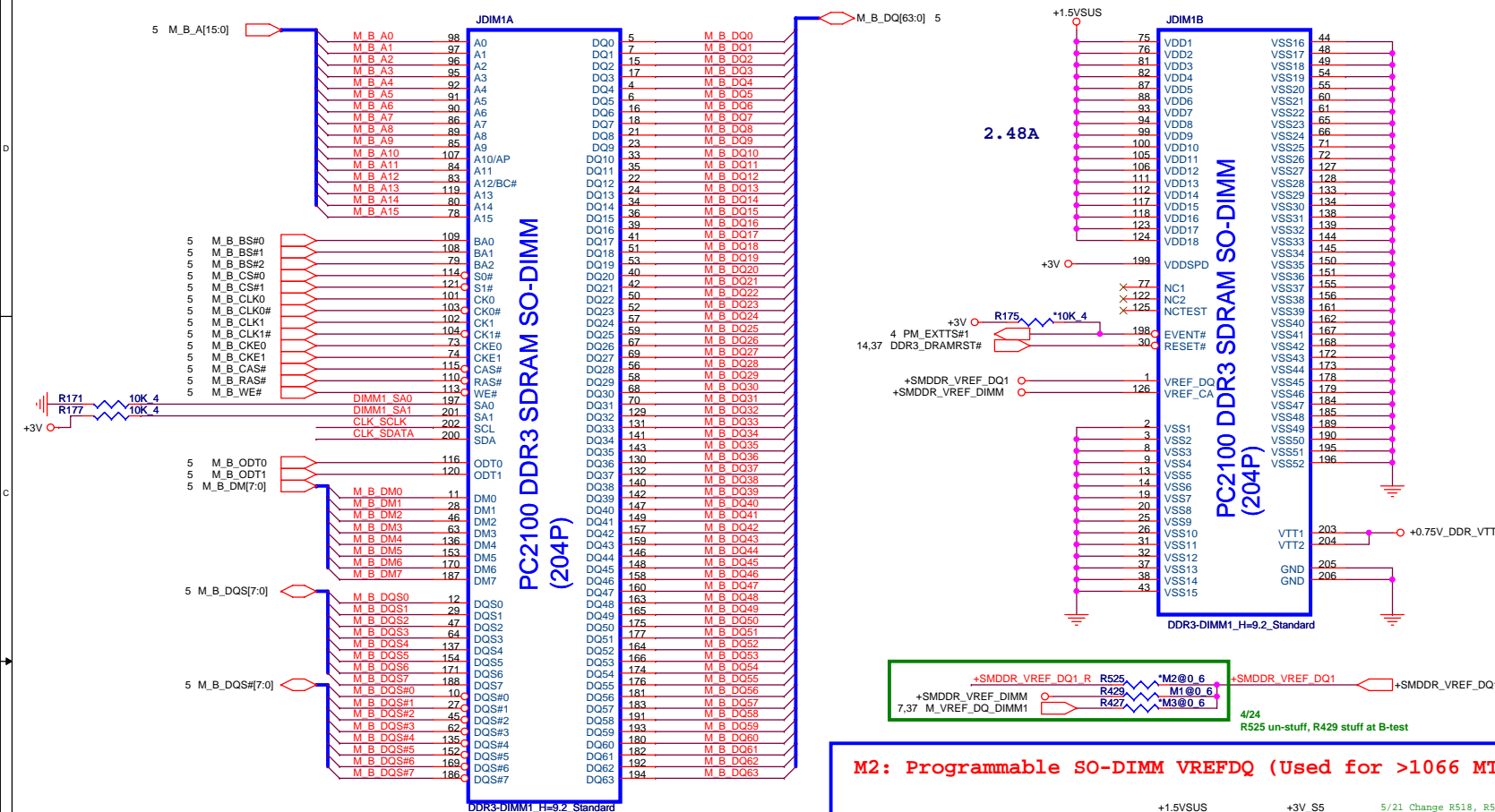
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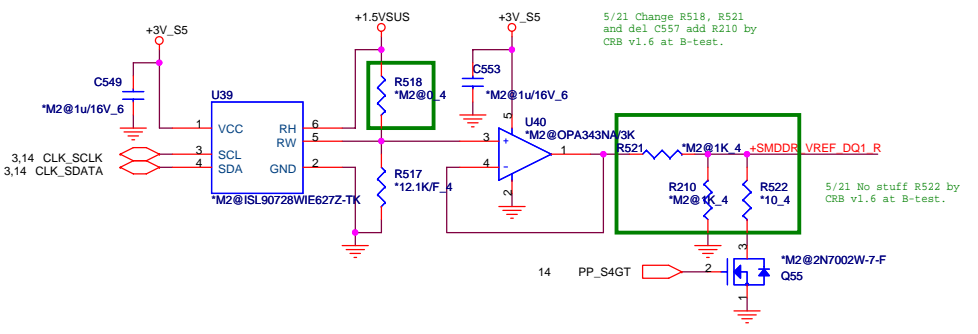
IBEX PEAK-M (GND)





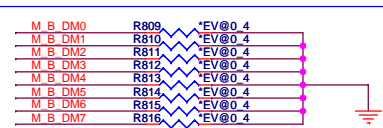


M2: Programmable SO-DIMM VREFDQ (Used for >1066 MT/s)



6/19 Reserve M2 component at C test.

6/22 Reserve R809-R816 at C test.



Close to SO-DIMM



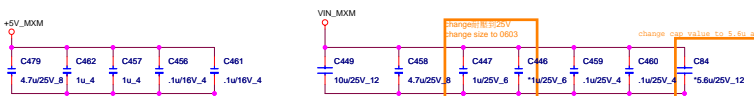
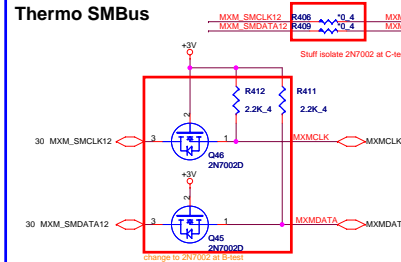
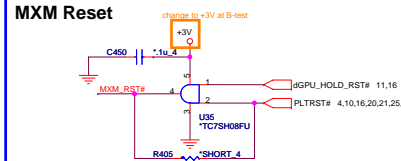
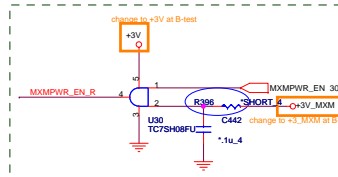
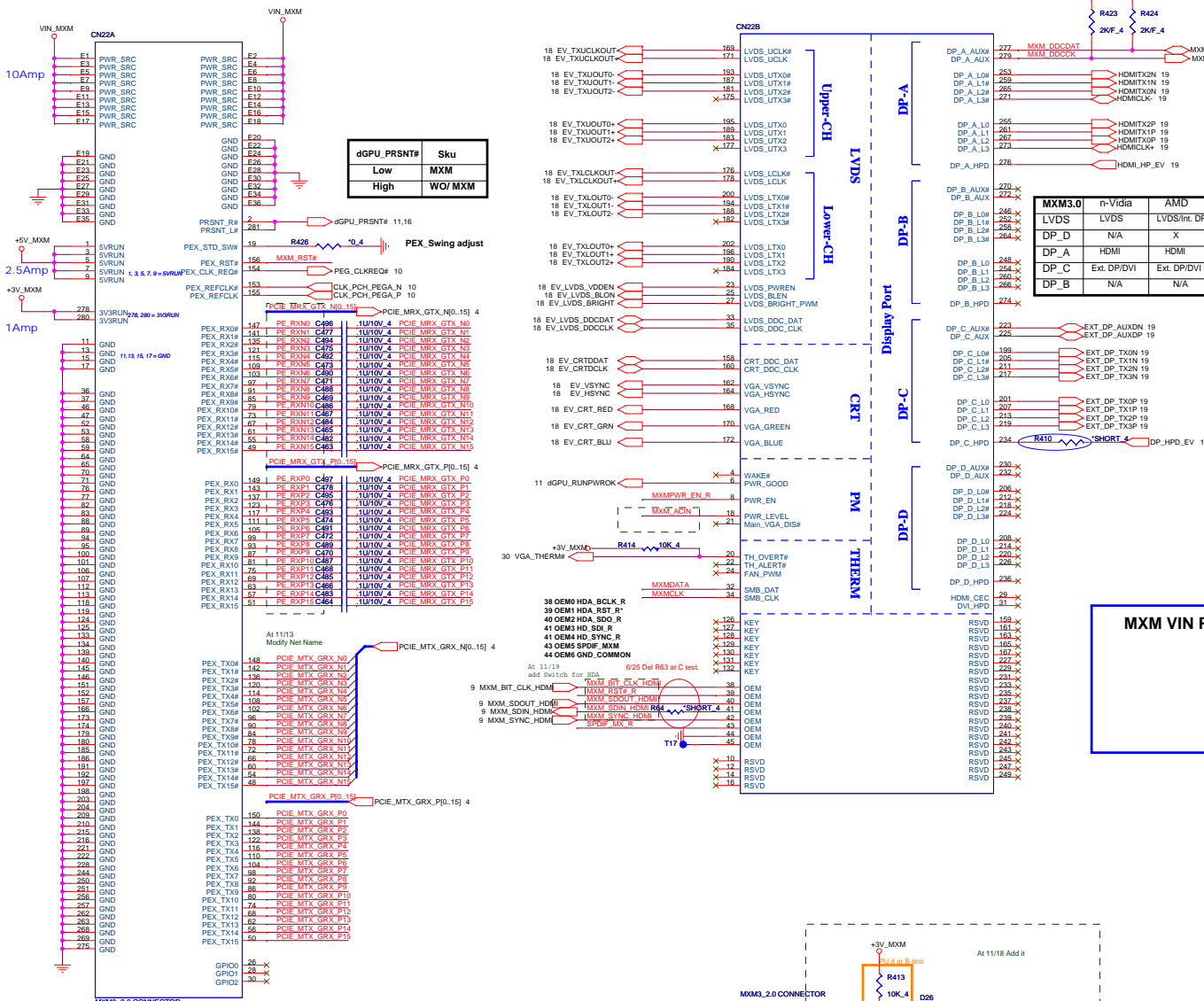
Quanta Computer Inc.

PROJECT : ZY9

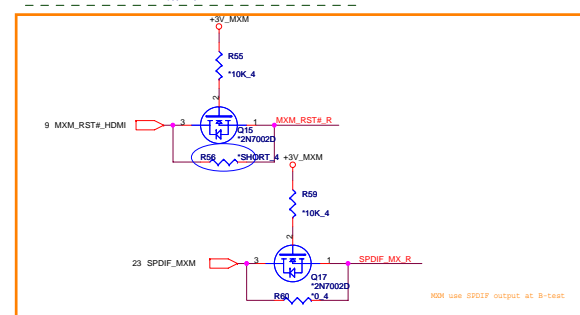
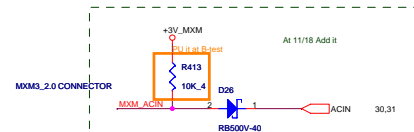
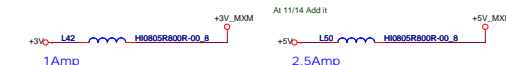
MXM Module

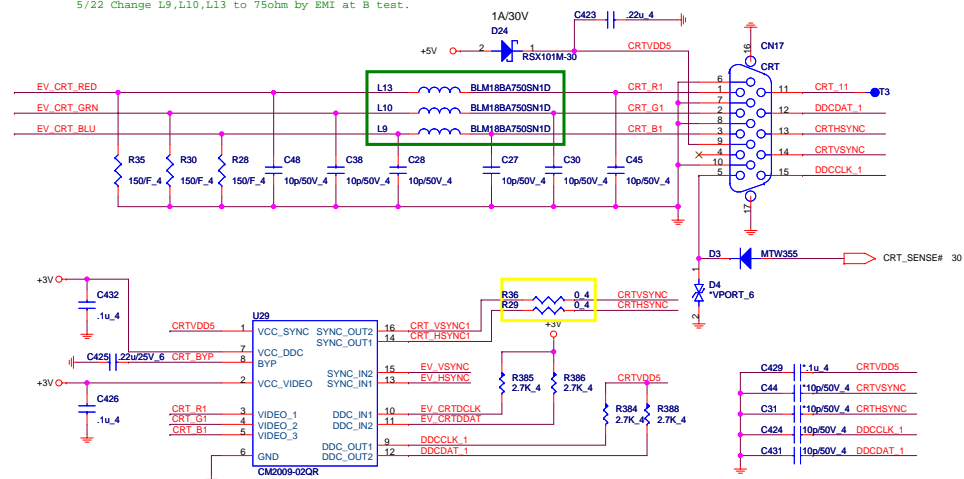
6/25 Change CN22 pin define and footprint at C test.

At 11/21
update MXM footprint to mxm-mm70-314-310b1-1-270p

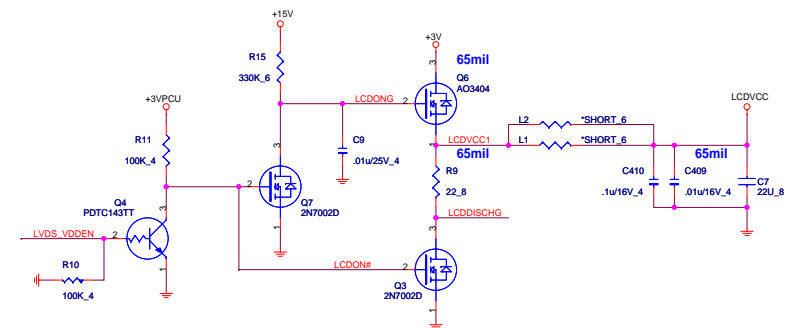
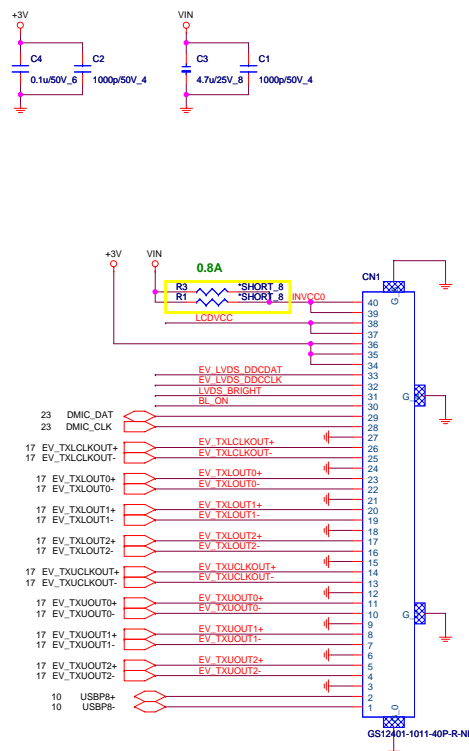


MXM 3V/5V Power switch

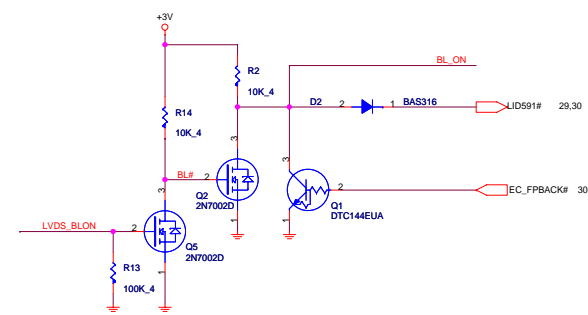




LCD Power



Backlight Control



HDMI **TMDS (DC-coupled)**
DP (AC-coupled)

17 HDMI1CLK- HDMI1CLK- C77 .1u_4
17 HDMI1CLK+ HDMI1CLK+ C80 .1u_4

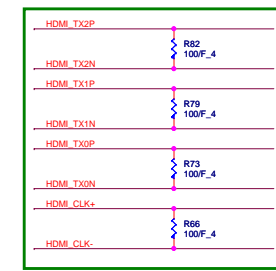
17 HDMI1TX0N HDMI1TX0N C83 .1u_4
17 HDMI1TX0P HDMI1TX0P C86 .1u_4

17 HDMI1TX1N HDMI1TX1N C87 .1u_4
17 HDMI1TX1P HDMI1TX1P C89 .1u_4

17 HDMI1TX2N HDMI1TX2N C90 .1u_4
17 HDMI1TX2P HDMI1TX2P C92 .1u_4

R86 499F_4
R83 499F_4
R81 499F_4
R78 499F_4
R76 499F_4
R69 499F_4
R67 499F_4
R65 499F_4

+3V 2 R92 Q20 2N7002D
100K_4

[illegible]

close to HDMI connector

U8

Pin	Signal	Pin	Signal
1	HDMI CLK	10	HDMI CLK
2	HDMI CLK	9	HDMI CLK
3	GND_3/8	8	GND_3/8
4	HDMI DDCCLK	7	HDMI DDCCLK
5	HDMI DDCDATA	6	HDMI DDCDATA

RClamp0524P

U10

Pin	Signal	Pin	Signal
1	HDMI TX2P	10	HDMI TX2P
2	HDMI TX2N	9	HDMI TX2N
3	GND_3/8	8	GND_3/8
4	HDMI TX1P	7	HDMI TX1P
5	HDMI TX1N	6	HDMI TX1N

RClamp0524P

U8

Pin	Signal	Pin	Signal
1	HDMI TX0P	10	HDMI TX0P
2	HDMI TX0N	9	HDMI TX0N
3	GND_3/8	8	GND_3/8
4	HDMI MB HP	7	HDMI MB HP
5		6	

RClamp0524P

DP Hot-PLUG to SB and GPU

DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

close to DP connector

U5

1	1	10	EXT DP1X3
2	2	10	EXT DP1X2P
3	3	10	EXT DP1X2N
4	GND_3/8	7	EXT DP1X3P
5	5	6	EXT DP1X3N

*RClamp0524P

U6

1	1	10	EXT DP1X3
2	2	10	EXT DP1X2P
3	3	10	EXT DP1X2N
4	GND_3/8	7	EXT DP1X3P
5	5	6	EXT DP1X3N

*RClamp0524P

U4

1	1	10	DP AUXP
2	2	10	DP AUXN
3	3	10	DP CAD
4	GND_3/8	7	DP HPD
5	5	6	DP HPD

*RClamp0524P

[illegible]

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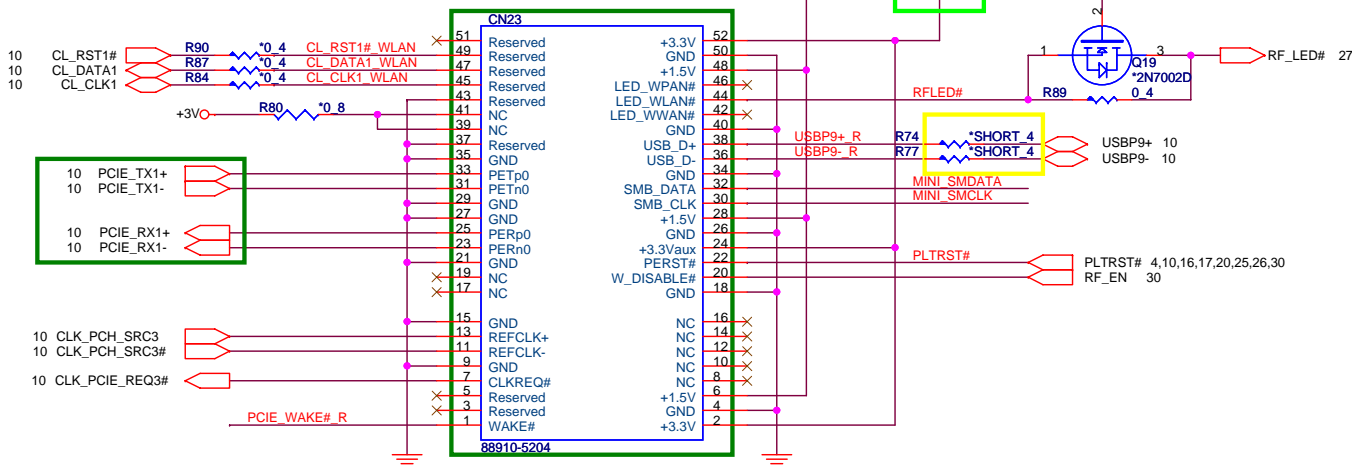
Size	Document Number	Rev
	LAN (BCM5764M/5784M)	3A
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Wireless

Modify to 2Conn. at B-test

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

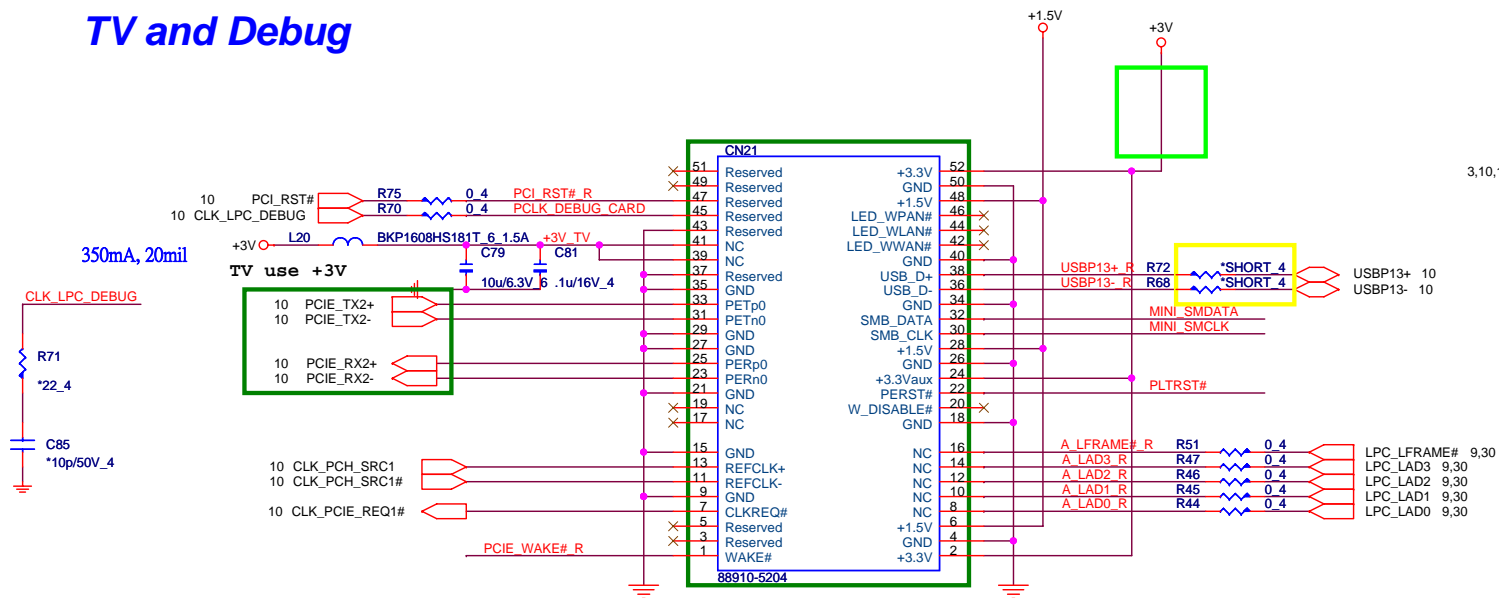
Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



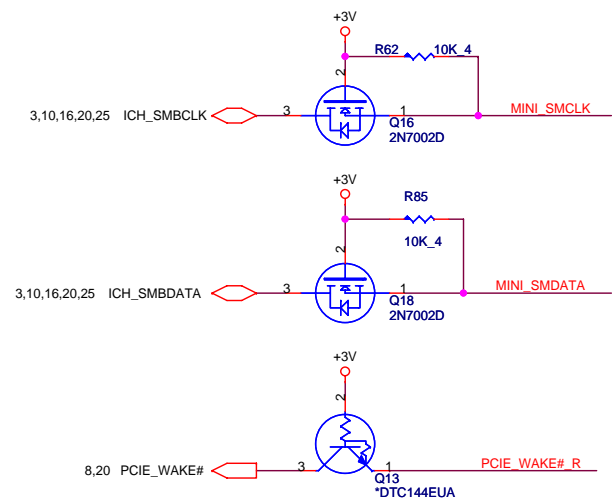
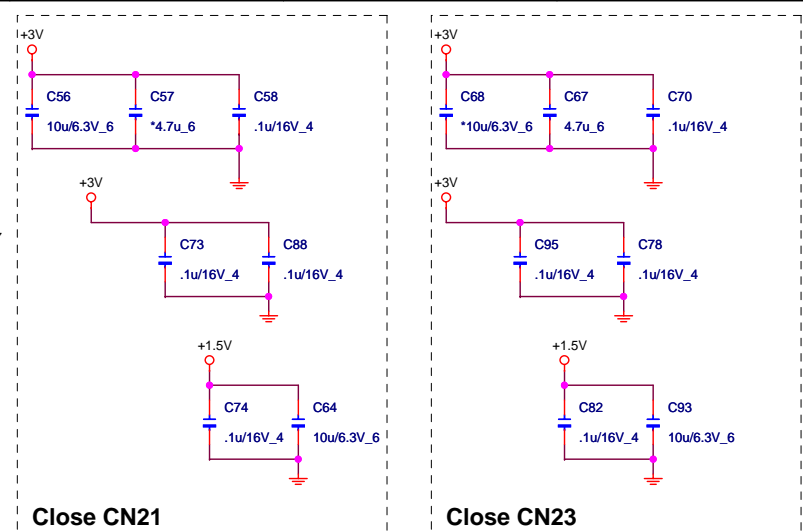
modify footprint at B-test
H=4


5/14 Change PCIE sequence between CN21 and CN23 by BIOS at B-test.

TV and Debug



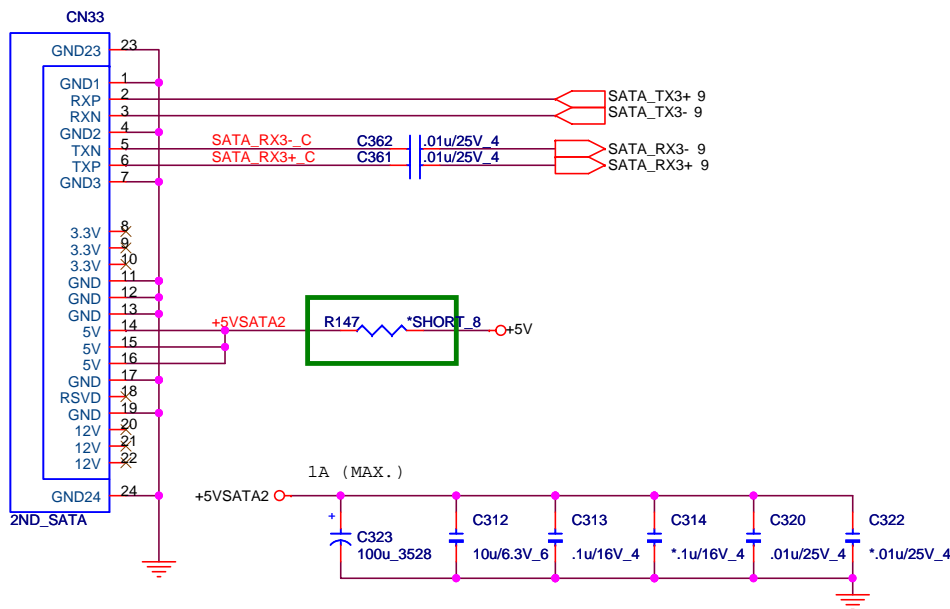
modify footprint at B-test
H=9



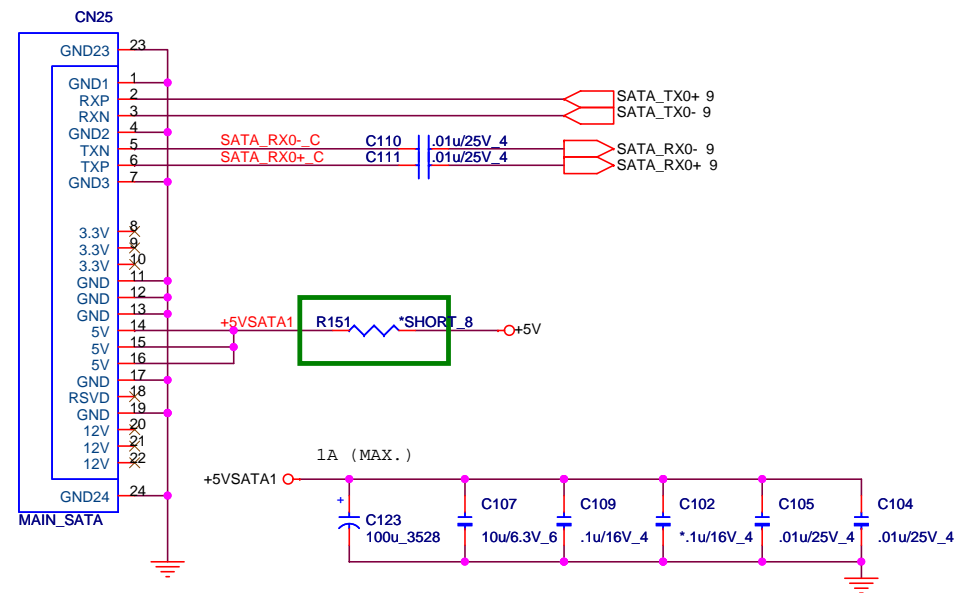
**Quanta Computer Inc.**
PROJECT : ZY9
MINI PCI-E card/TV

Size	Document Number	Rev
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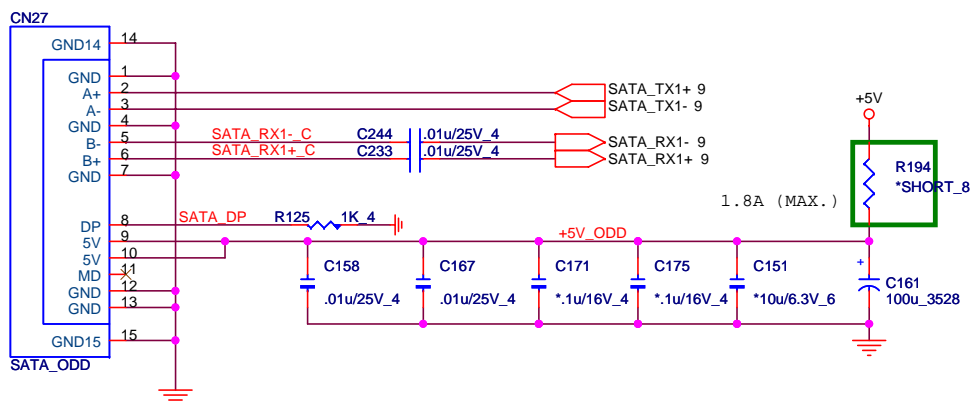
2nd SATA HDD (edge of board)



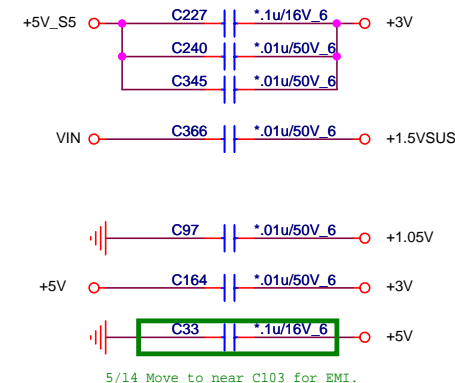
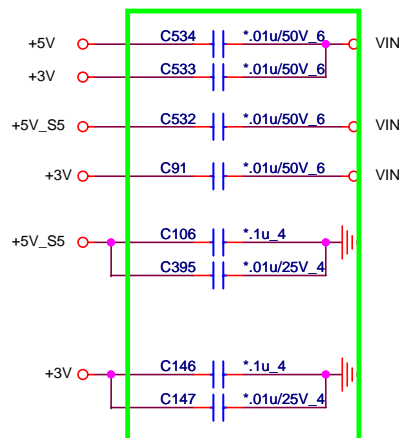
MAIN SATA HDD




ODD (SATA)



EE RETURN-PATH CAPACITORS

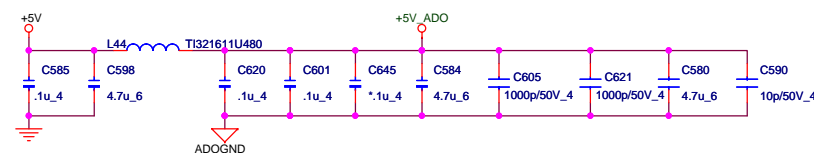


 Quanta Computer Inc. PROJECT : ZY9		Size	Document Number	Rev
				3A
SATA-HDD/ODD		Date:	Thursday, August 27, 2009	Sheet 22 of 42

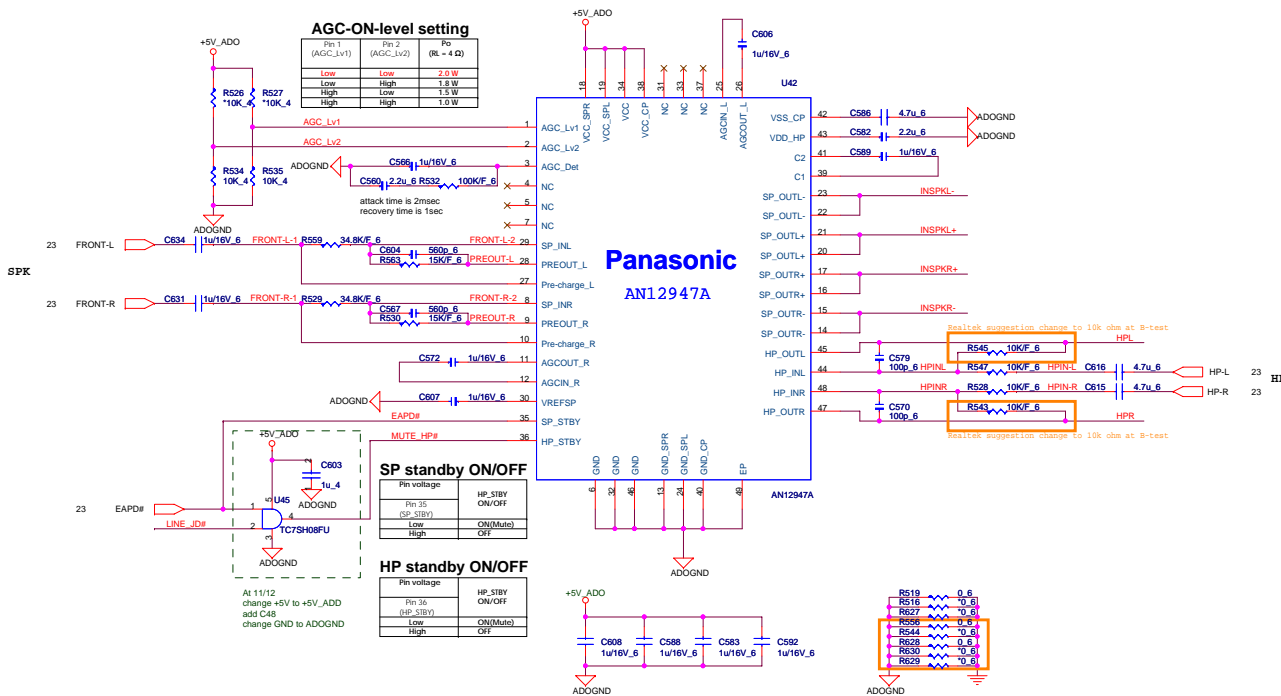
IV@
EV@



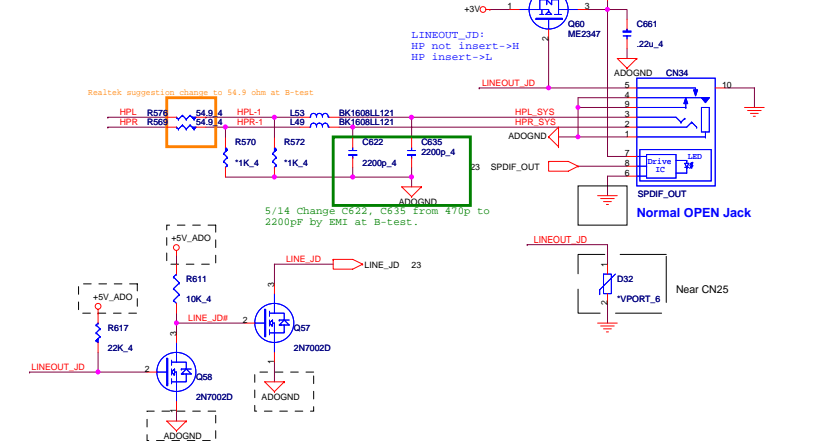
5/11: Add U50, C666 and R561 for Po issue at B-test



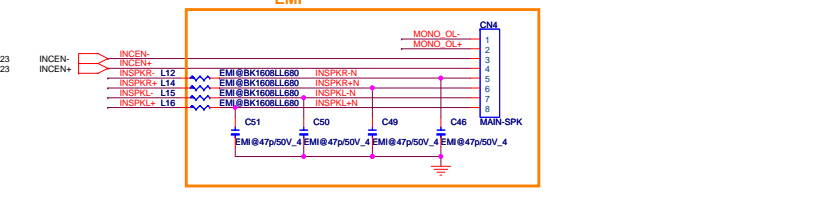
SPEAKER/HP AMP.



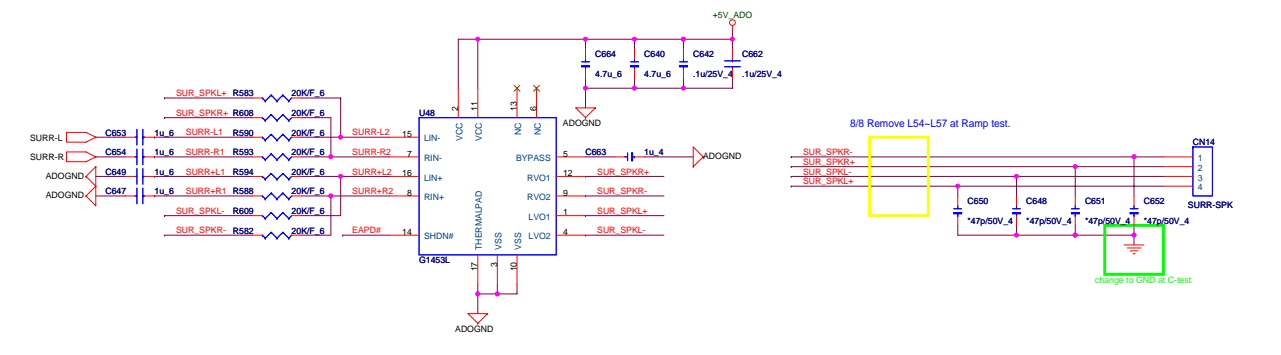
LINE-OUT/SPDIFO



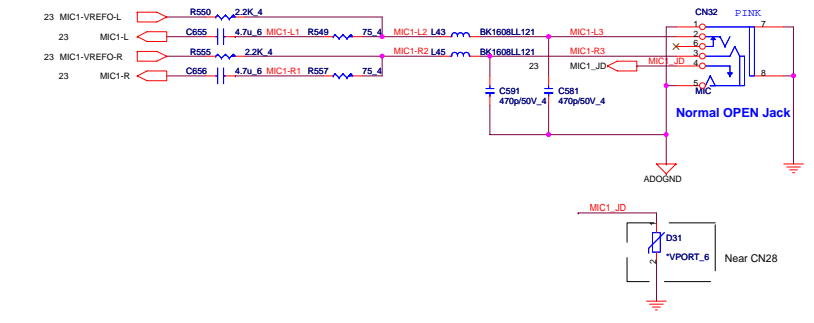
Main SPK/Center/Subwoofer



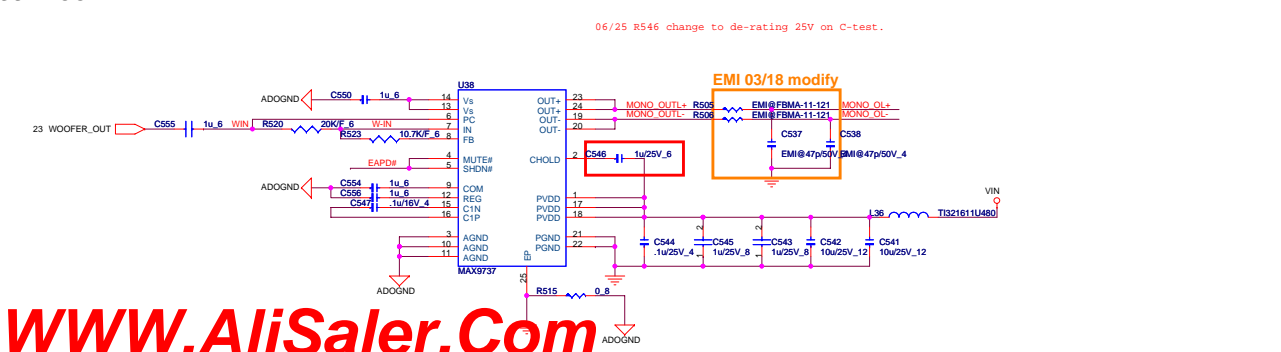
SURR-SPK



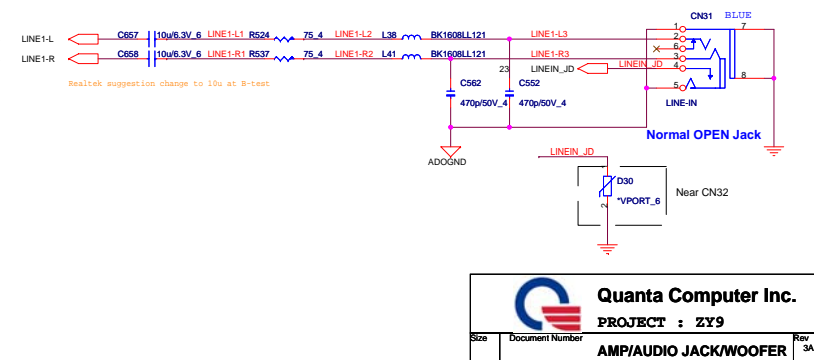
MIC



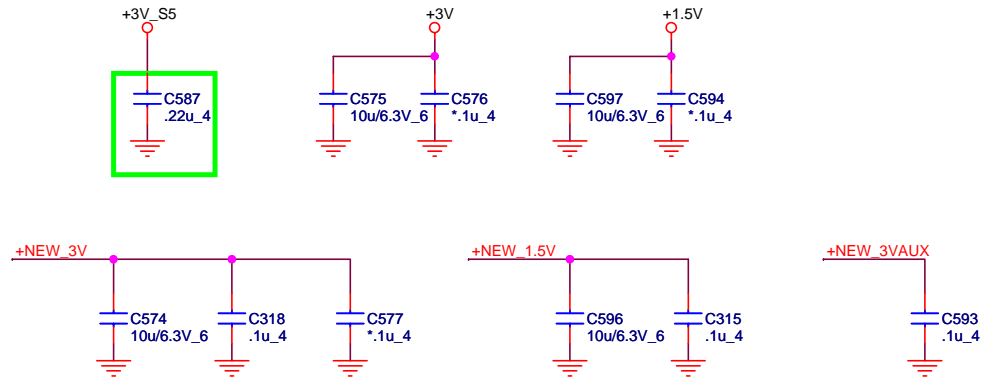
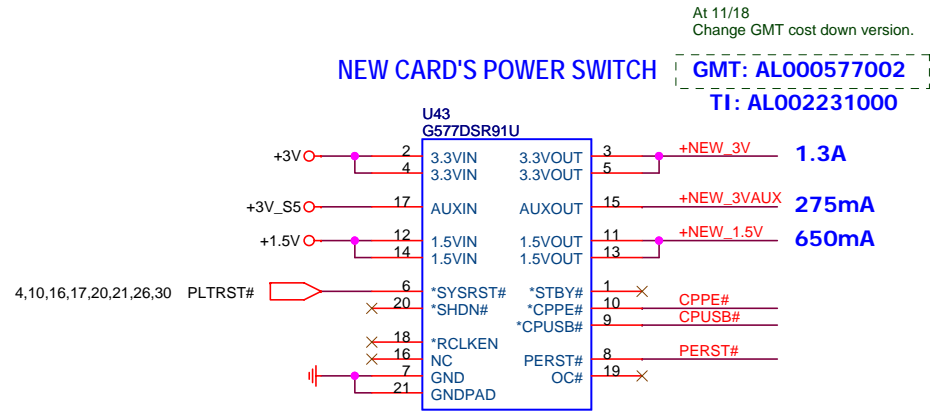
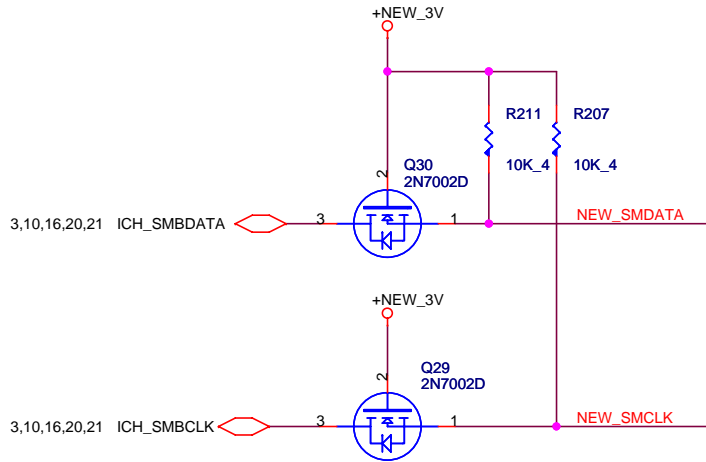
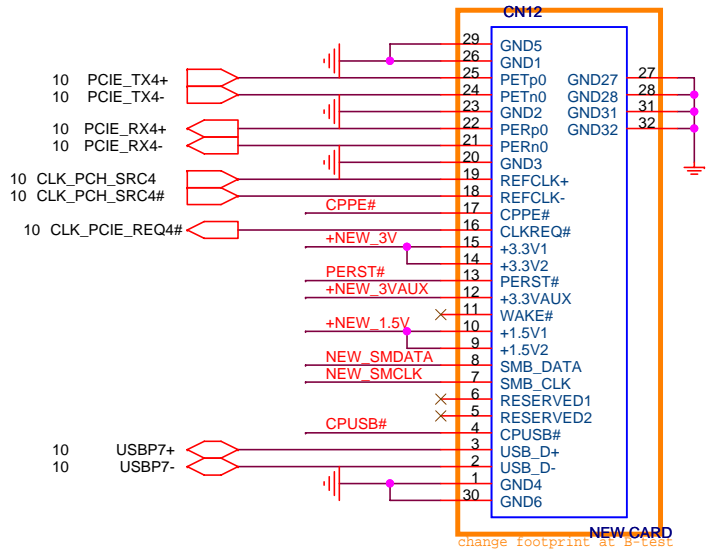
SUBWOOFER



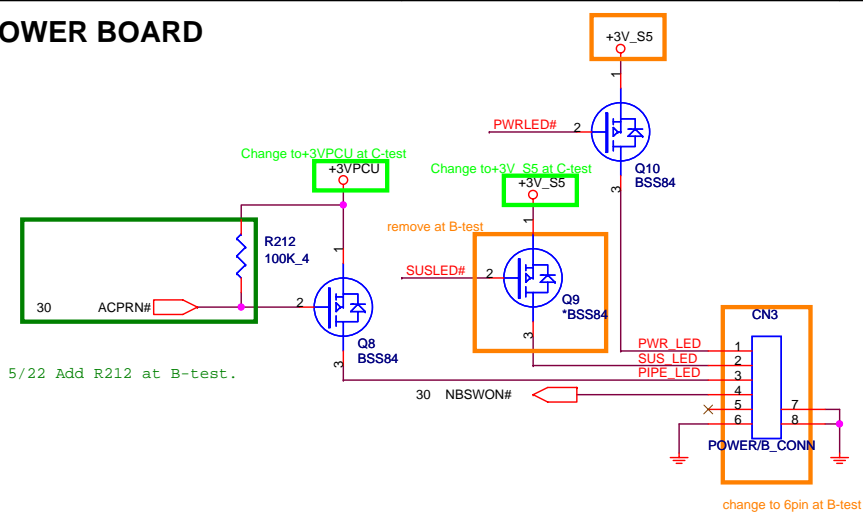
LINE IN



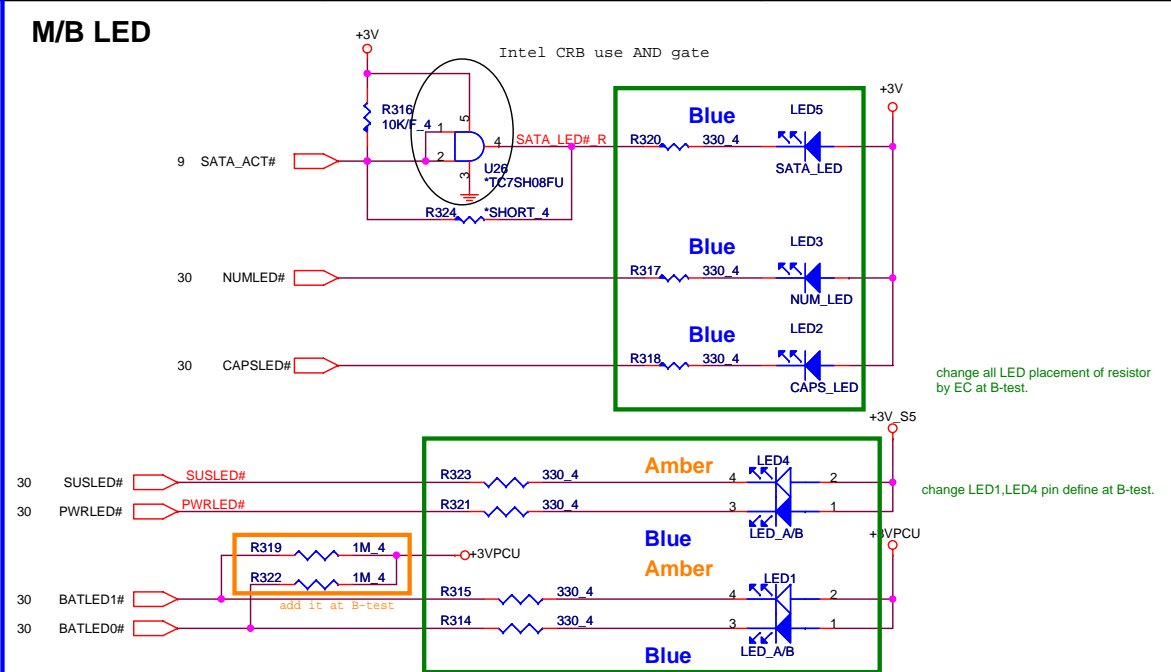
NEW CARD



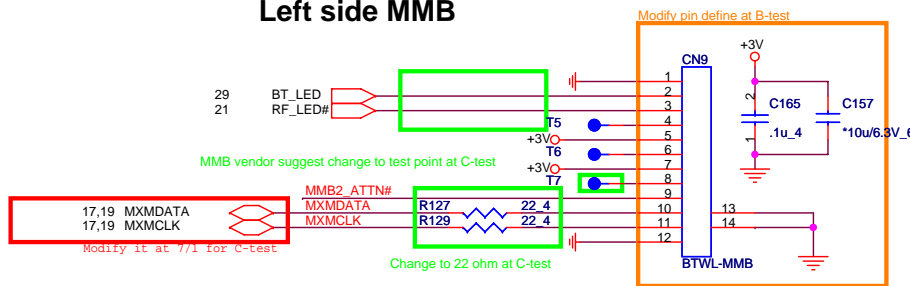
POWER BOARD



M/B LED

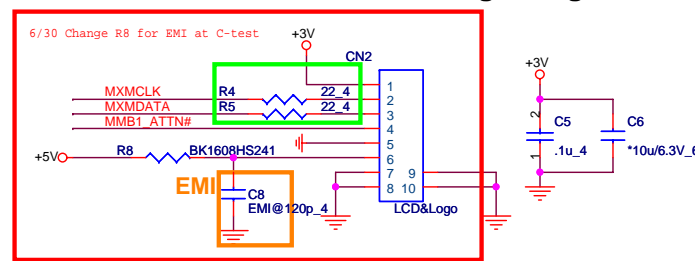


Left side MMB

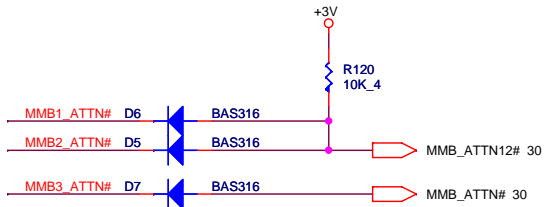


MXMCLK=MXM_SMCLK; MXMCDATA=MXM_SMDATA12
MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.

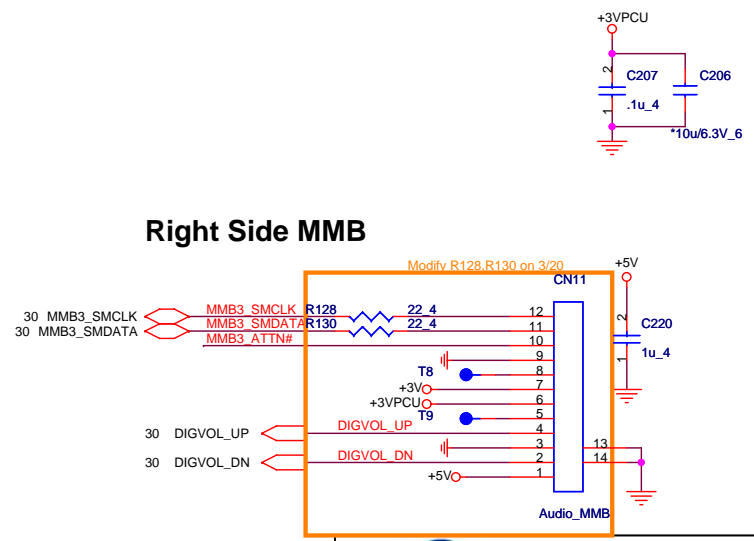
LCD BL_ON/OFF MMB & Backlight Logo LED



MMB Status



Right Side MMB

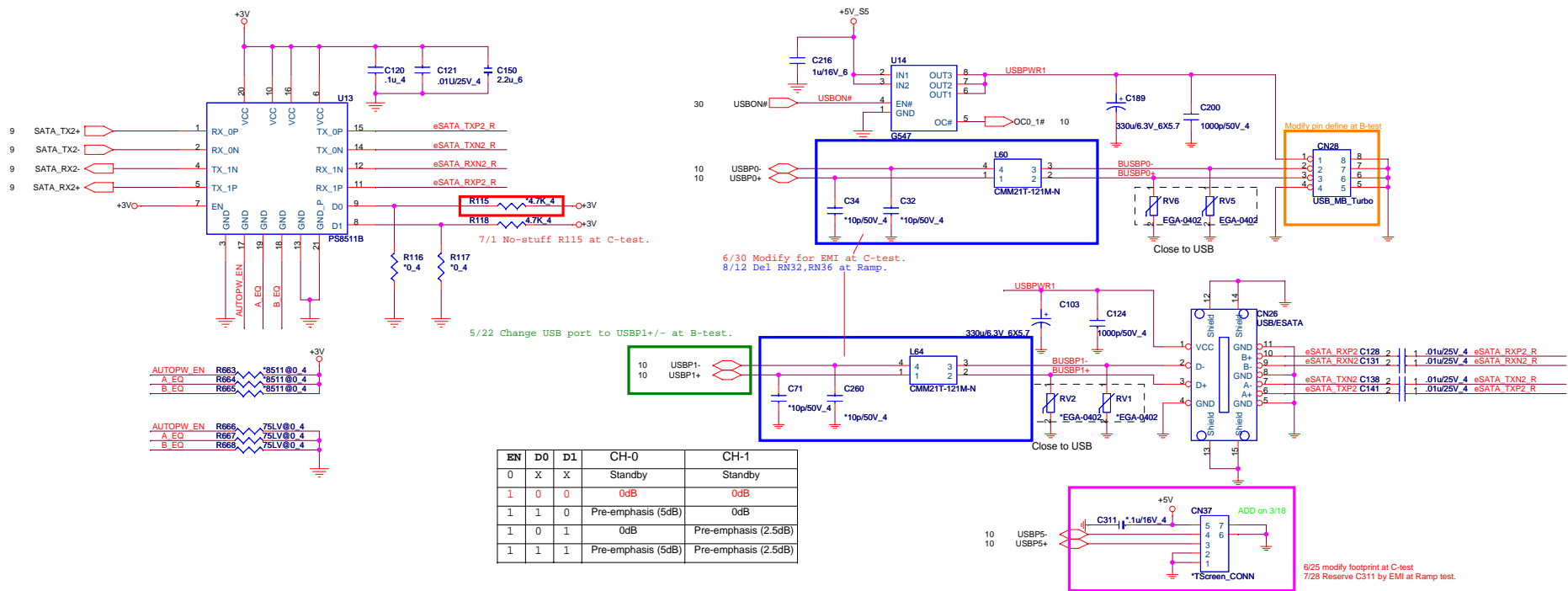


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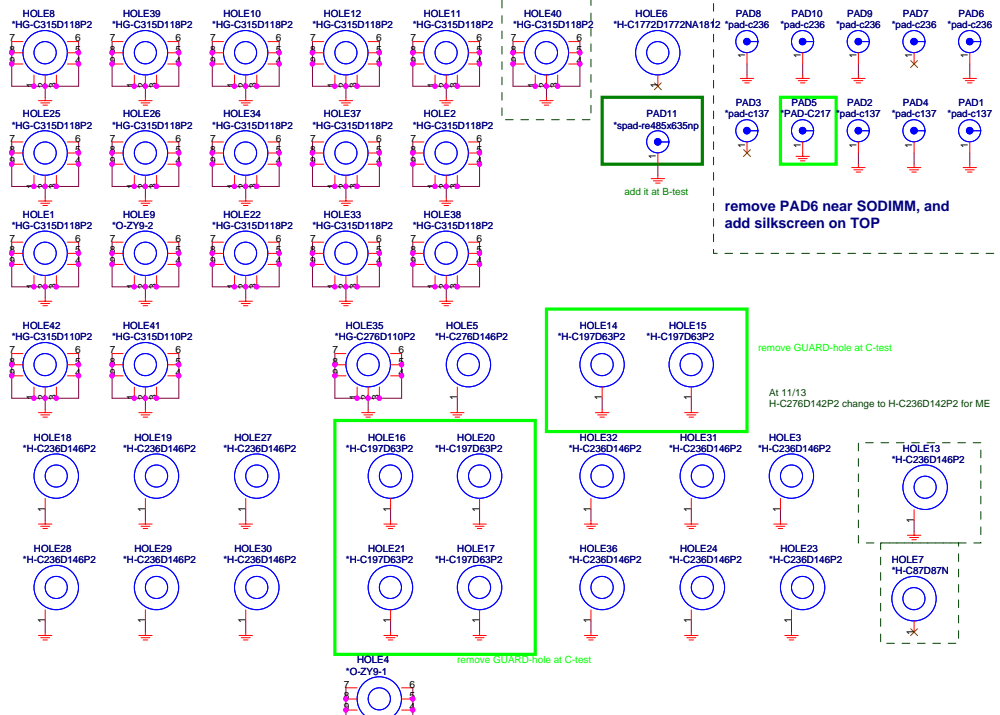
PROJECT : ZY9

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	3A
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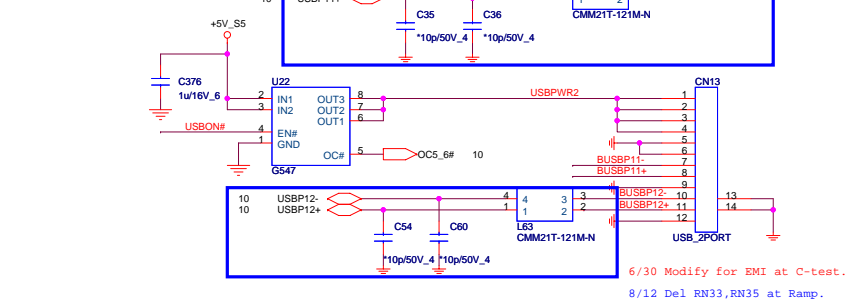
USB & ESATA



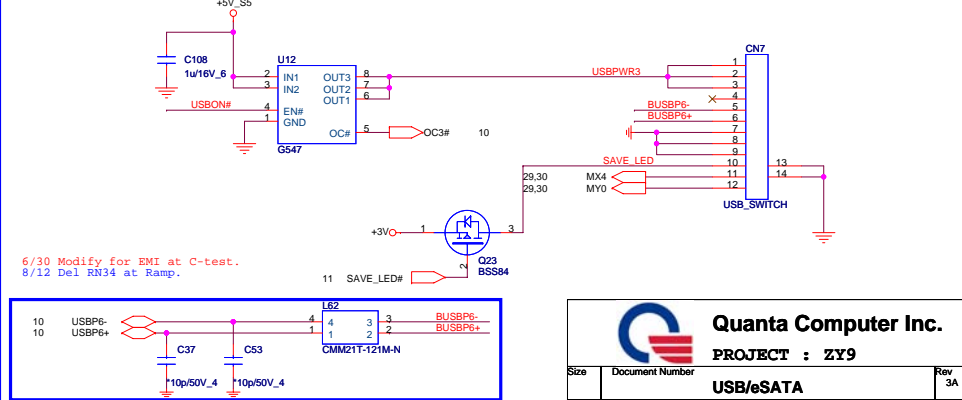
HOLES



USB_2PORT/B

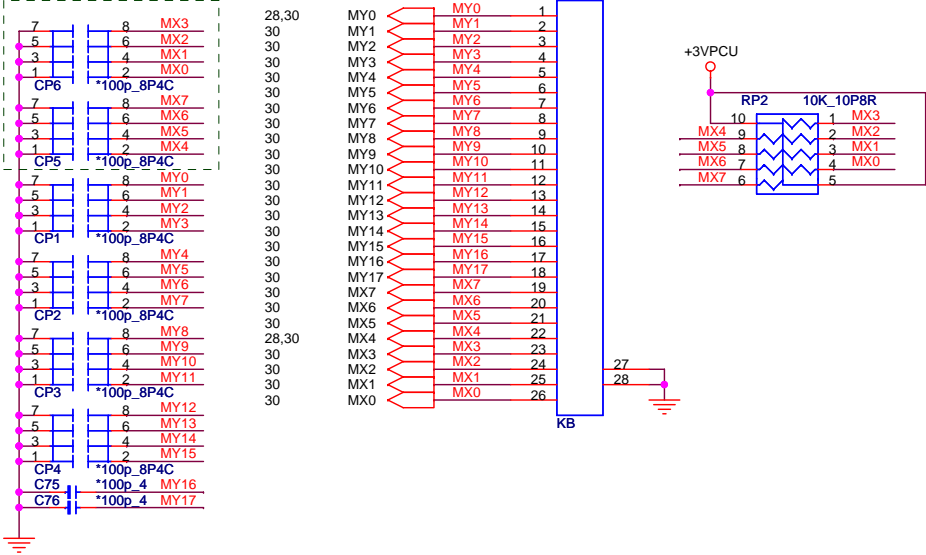


USB_SWITCH/B

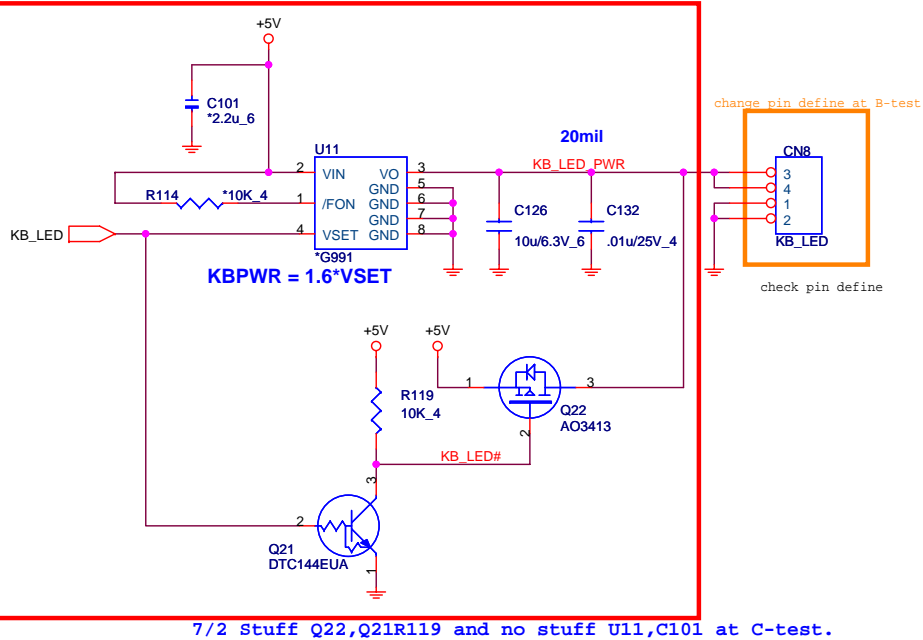


INT K/B

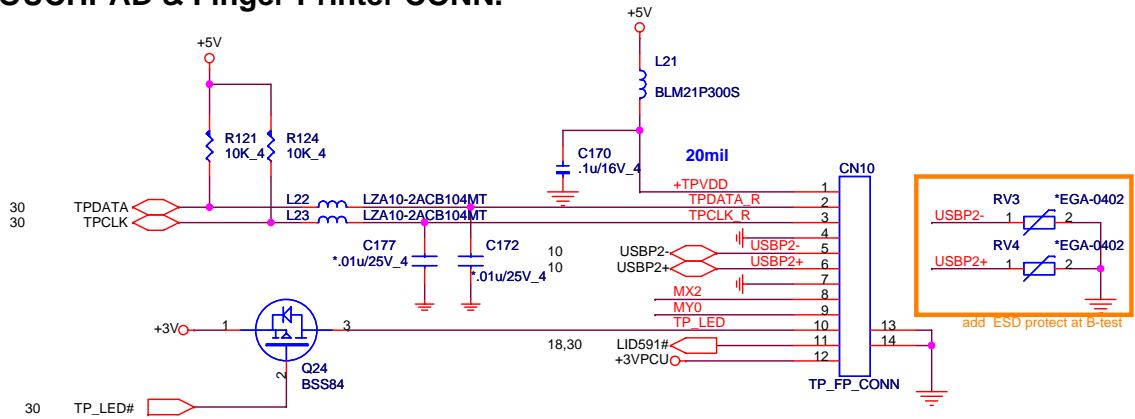
At 11/18
SWAP



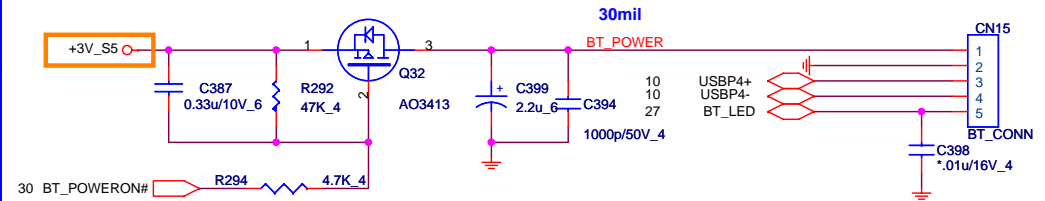
Keyboard LED control



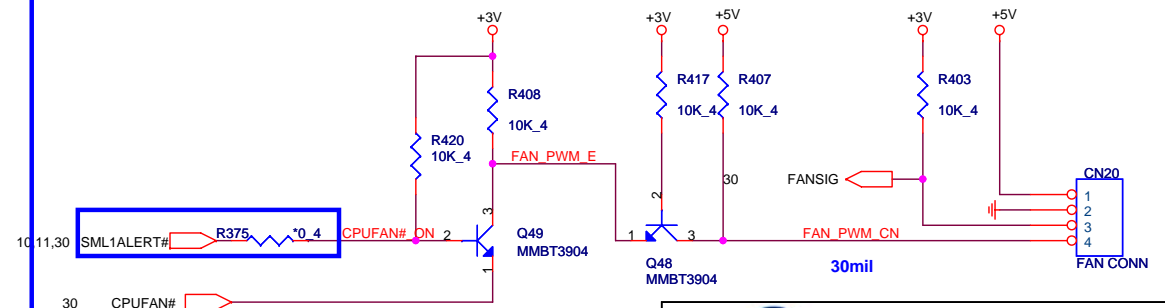
TOUCHPAD & Finger-Printer CONN.



BLUETOOTH CONNECTOR



CPU FAN



5/13 Reserve R375 by EC at B-test.

6/25 Stuff R375 by EC at C-test.

7/22 Un-stuff R375 by EC at Ramp.

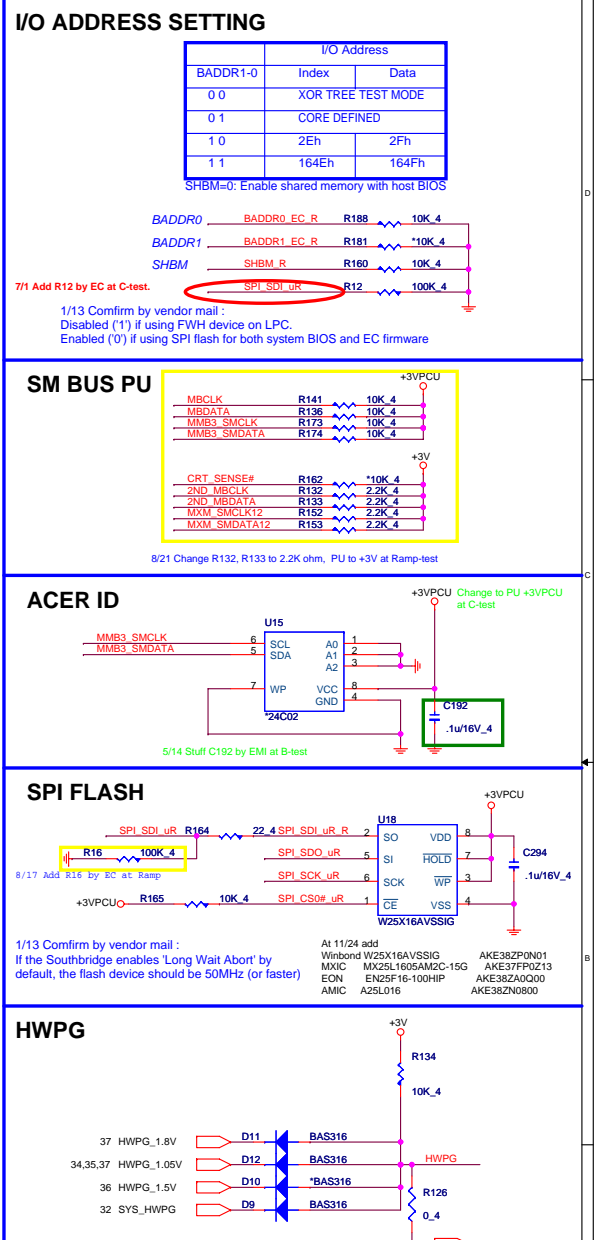
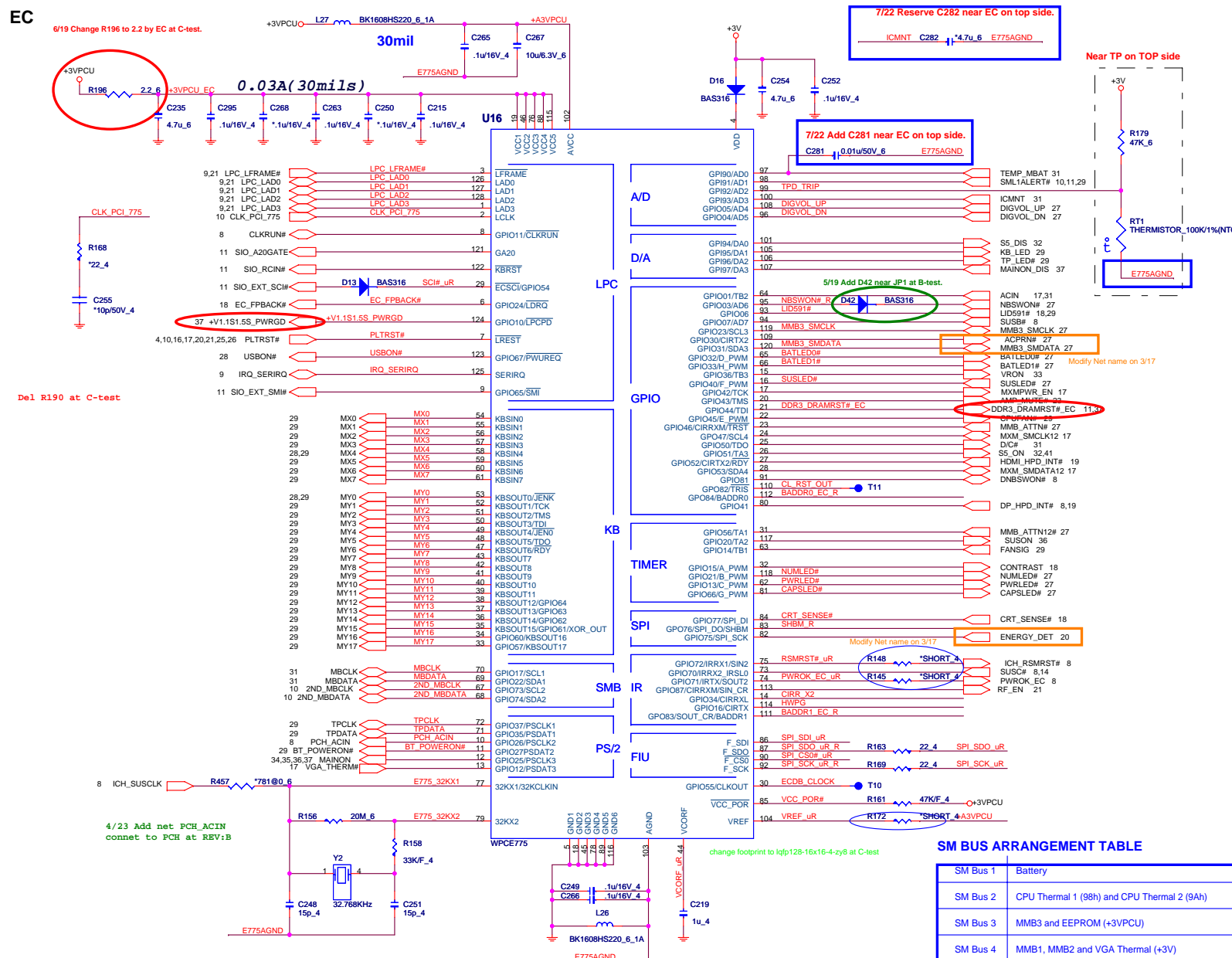


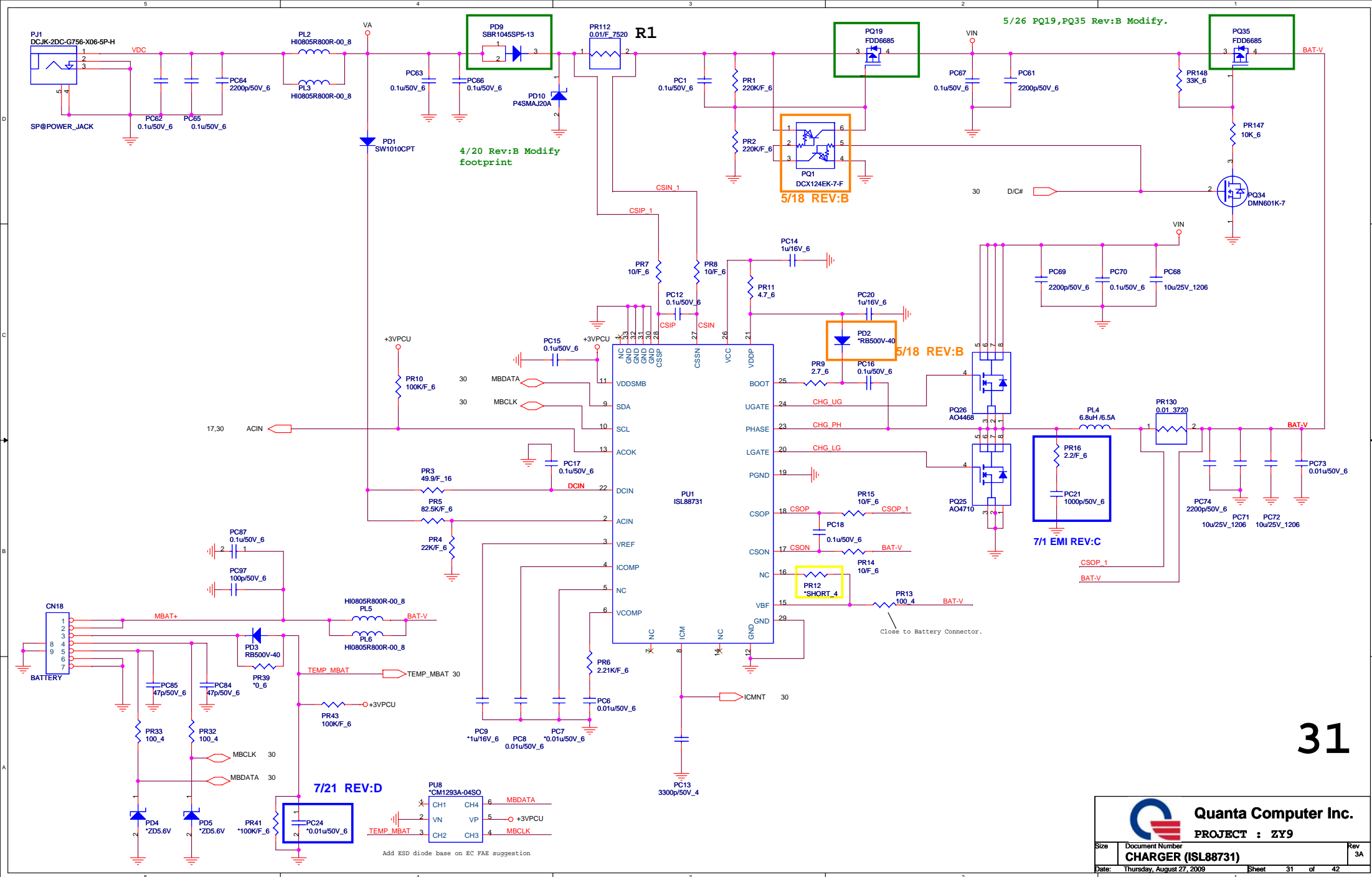
Quanta Computer Inc.

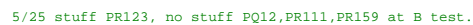
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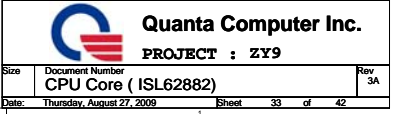
KB/FAN/TP+FP/BT

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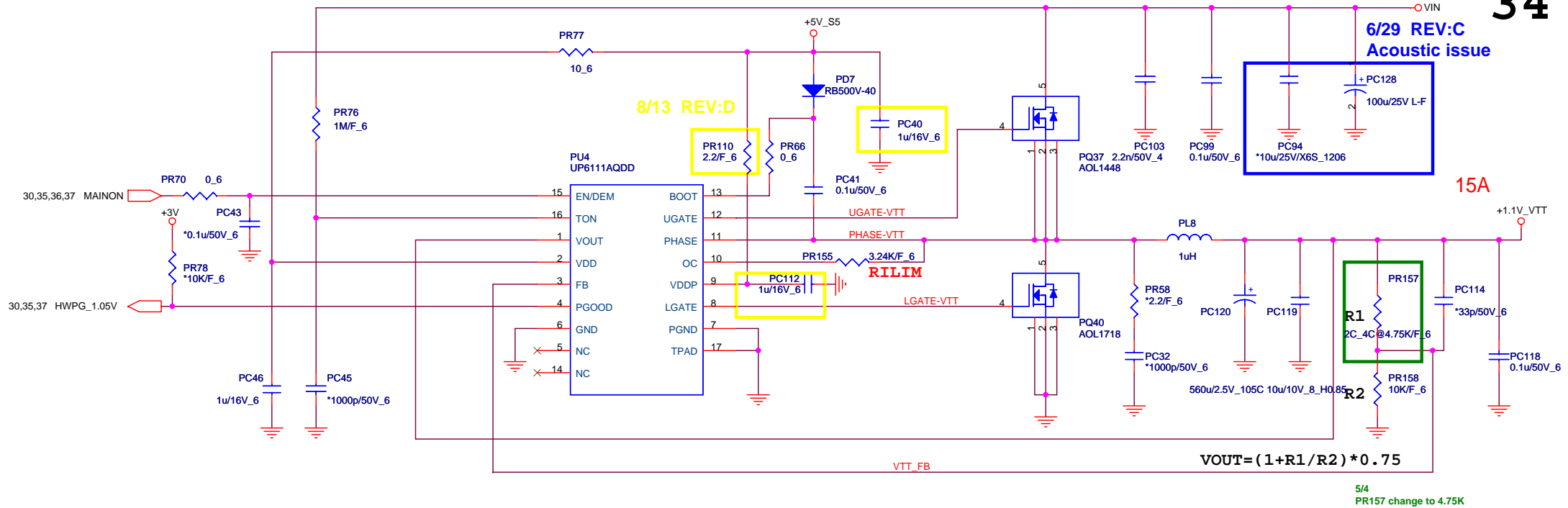






6/29 REV:C
Acoustic issue

15A

AO1718 $R_{dson} = 3 \sim 4.3m\Omega$ Aurbundale (1.05V) $R1 = 4.02K$ (CS24023F928)Clarksfield(1.1V) $R1 = 4.75K$ (CS24753F919)

$L(\text{ripple current})$
 $= (19 - 1.05) * 1.05 / (1\mu * 272k * 19)$
 $\sim 3.64A$

$4.3m * 15 = RILIM * 20\mu A$
 $RILIM = 3.24K$ (3.22K)

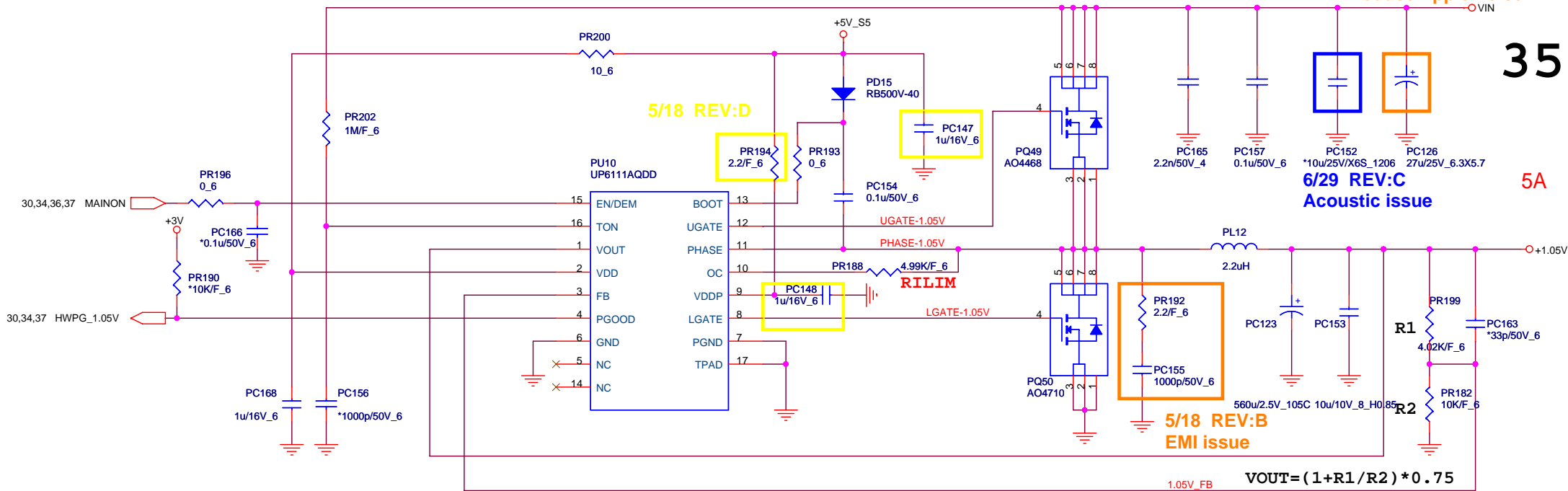


Quanta Computer Inc.

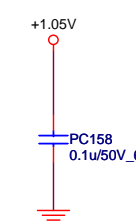
PROJECT : ZY9

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[PWM]



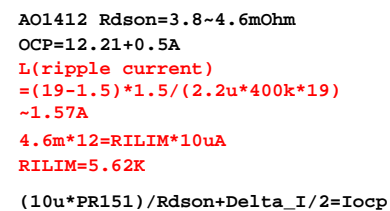
AO4710 $R_{dson} = 11.8 \sim 14.2 \text{m}\Omega$
 OCP = 7.2-0.8A
 $L(\text{ripple current})$
 $= (19 - 1.05) * 1.05 / (2.2\mu * 272k * 19)$
 $\sim 1.6577A$
 $14.2m * 7 = RILIM * 20\mu A$
 $RILIM = 4.99K (4.97K)$

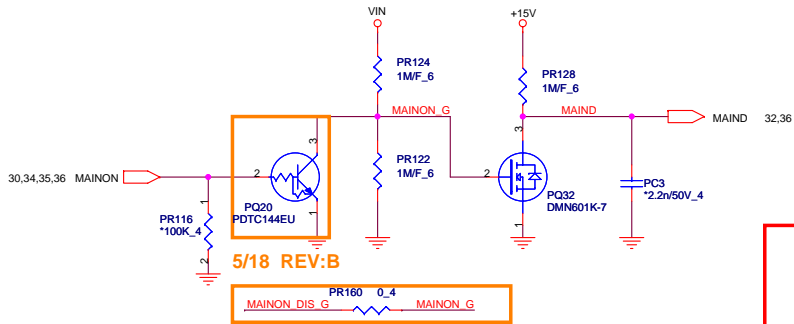
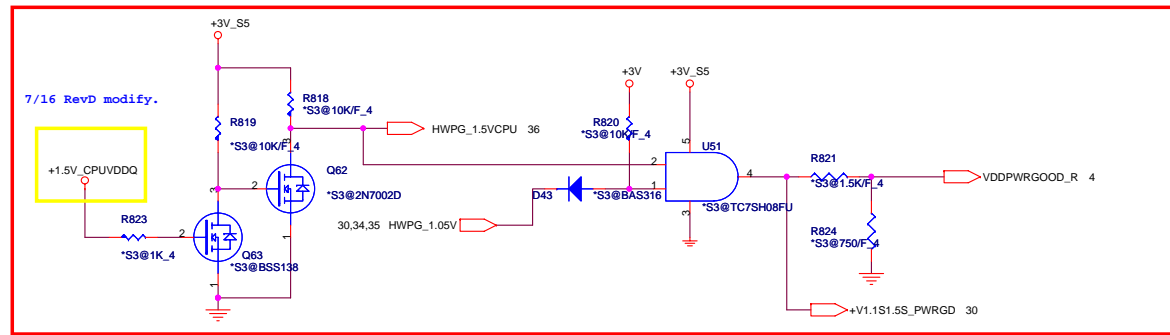


Quanta Computer Inc.

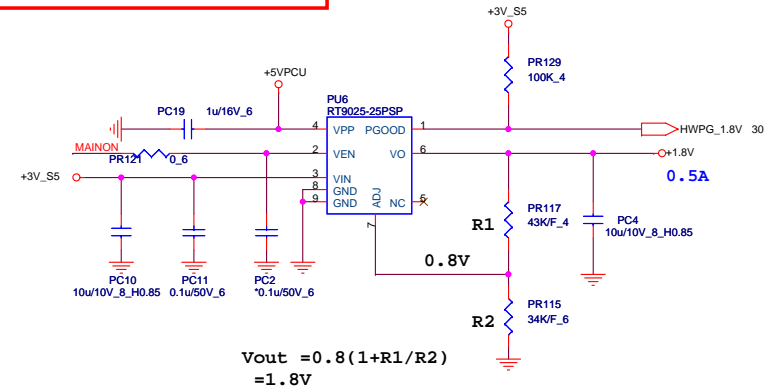
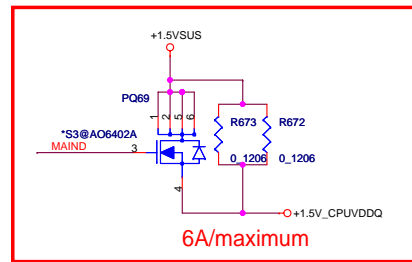
PROJECT : ZY9

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5/25 stuff PR160, no stuff PQ24, PR126, PR125 at B test.



S3 power solution: C277~C280 stuff 0.1uF cap;
Normal : Stuff 0ohm to short.

